(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 574 137 A1**

(12) **EUROPEAN PATENT APPLICATION**

(21) Application number: **93303657.6**

(22) Date of filing: **12.05.93**

(51) Int. Cl.^{5}: **H01L 27/12**, G02F 1/136, H01L 29/784

(30) Priority: **13.05.92 JP 120699/92**
19.08.92 JP 220503/92

(43) Date of publication of application:
15.12.93 Bulletin 93/50

(84) Designated Contracting States:
DE FR GB

(71) Applicant: **SEIKO INSTRUMENTS INC.**
31-1, Kameido 6-chome Koto-ku
Tokyo 136 (JP)

(72) Inventor: **Takahashi, Kunihiro**
c/o Seiko Instruments Inc., 31-1 Kameido 6-chome
Koto-ku, Tokyo (JP)

Inventor: **Kojima, Yoshikazu**
c/o Seiko Instruments Inc., 31-1 Kameido 6-chome
Koto-ku, Tokyo (JP)
Inventor: **Takasu, Hiroaki**
c/o Seiko Instruments Inc., 31-1 Kameido 6-chome
Koto-ku, Tokyo (JP)
Inventor: **Yamazaki, Tsuneo**
c/o Seiko Instruments Inc., 31-1 Kameido 6-chome
Koto-ku, Tokyo (JP)
Inventor: **Iwaki, Tadao**
c/o Seiko Instruments Inc., 31-1 Kameido 6-chome
Koto-ku, Tokyo (JP)

(74) Representative: **Sturt, Clifford Mark et al**
J. MILLER & CO. 34 Bedford Row Holborn
London WC1R 4JH (GB)

(54) **Semiconductor device.**

(57) A semiconductor device is formed using a monosilicon (2) substrate laminated to a temporary substrate through an insulator (1). An integrated circuit (10,11) is formed on the monosilicon. The monosilicon is then fixed to a support member (6) through an adhesive (5) and protective films (3, 4, 7).

The device has a number of features to improve the reliability thereof including:

a) that the protective film comprises silicon oxynitride or silicon nitride (3);

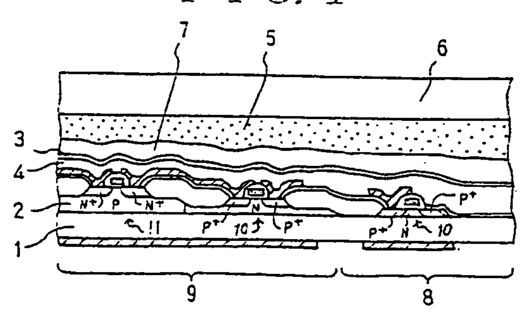
b) a levelling layer (7);

c) spacing the bottom of the source and drain regions in a transistor in the integrated circuit from the insulator; and

d) doping near the channel to suppress any parasitic channel.

The semiconductor device has particular application as a drive substrate for a light valve in an active matrix.

FIG. 1



1 dielectric material
2 monosilicon layer
3 silicon oxynitride film or silicon nitride film
5 adhesive layer
6 support member
7 leveling layer
8 pixel switching element group
9 driver integrated circuit

EP 0 574 137 A1

The present invention relates to a semiconductor device. Particularly but not exclusively, the present invention relates to a semiconductor drive substrate used for a light valve such as an active matrix liquid crystal display. More specifically, the present invention relates to a structure in which a pixel switching element group and a peripheral driver circuit are formed integrally on a common substrate.

Conventionally, a so-called TFT substrate in which thin film transistors (TFT) are integrally formed on an insulating substrate, such as quartz, have been known to constitute a drive substrate of an active matrix light valve. For example, Japanese Patent Laid-open No. 3-101714 discloses a TFT substrate utilizing polysilicon as a semiconductor thin film material. Furthermore, it is also known to employ another type of TFT substrate utilizing an amorphous silicon in place of the polysilicon. In either case, the polysilicon and amorphous silicon have a relatively small carrier mobility: hence it is difficult to form a peripheral drive circuit on the same substrate.

Recently, other technology has been developed and is disclosed in, for example, Japanese Patent Laid-open No. 3-100516. In this other technology, a single crystal silicon or monosilicon layer is laminated on an insulating substrate, such as quartz, to form the drive substrate. In contrast to polysilicon and amorphous silicon, monosilicon has a relatively great mobility, and therefore has an advantage that a peripheral drive circuit of high performance and large capacity may be formed concurrently by utilizing regular IC fabrication processes. However, in practice the process temperature during IC fabrication can reach up to 1150°C, which causes bending deformation of a wafer due to the difference of thermal expansion coefficients between the monosilicon layer and the insulating substrate. This results in the drawback that the desired yield rate cannot be obtained.

Another technology which has been recently developed involves a drive substrate of the light valve formed of a bulk monosilicon wafer, as disclosed, for example, in 8th International Workshop on Future Electron Devices, March 14 - 16, 1990, pages 81 - 84, Kouch-Ken, Japan. Regular LSI fabrication processes can be applied to the bulk monosilicon wafer without problems. However, the wafer must be transformed into a transparent substrate for use in the light valve. An integrated circuit formed in the wafer is subjected twice to a device transfer process, so as to replace the silicon wafer by a transparent substrate, thereby disadvantageously complicating the fabricating steps.

In order to reduce the number of steps for device transfer in changing the bulk monosilicon wafer to a transparent substrate, in the prior art one has used epitaxial technology which is disclosed, for example, in Japanese Patent Laid-open Nos. 63-90859 and 63-101831. In this prior art, an insulating layer is formed on a surface of a single crystal silicon wafer, and thereafter a window is selectively opened to form therein an epitaxial monosilicon region. A transistor device is formed in this epitaxial region, and then the transistor device is transferred to a transparent substrate to thereby replace the silicon wafer. In this transferring process, the surface of the transistor device is coated by a protective film composed of silicon dioxide by chemical vapour deposition CVD, and further the transparent substrate is laminated by an adhesive. Then, the bulk portion of the silicon wafer is removed while utilizing the above mentioned insulating film as an etching stopper.

In the last mentioned prior art (JP-A-63-101831), the regular IC fabrication process is applicable since the monosilicon wafer is utilized, and further advantageously only a single device transfer process is required. However, when transferring the integrated transistor device, the silicon wafer and the transparent substrate or a support member are laminated with each other by adhesive. The adhesive normally contains contaminants such as alkali metal: hence the device surface is provisionally applied with a protective film or a passivation film. As described before, the protective film is composed of a silicon dioxide film containing phosphorus (PSG film) deposited by CVD. However, the adhesive contains water vapor and hydrogen gas besides the alkali metal, which may disadvantageously degrade the electrical characteristics of the device. While the PSG film can effectively block contaminants such as alkali metal, the water vapor and hydrogen gas may permeate the PSG film, therefore failing to protect the device.

In view of the problems of the prior art, a first object of the present invention is to prevent degradation of the device and to improve the reliability in the substrate structure where a light valve device formed on the monocrystal semiconductor layer is transferred to the transparent support member.

Further, in the above last noted prior art (JP-A-63-101831), the surface of the monosilicon wafer is covered by the insulating film, which is then selectively opened to provide a window to form an epitaxial region for integrating the device. However, such a process is rather complicated, requires delicate control and is therefore not suitable for mass production.

In view of this, according to the present invention, a drive substrate of an active matrix light valve is formed by using a substrate having a monosilicon layer disposed on a silicon wafer through an electrically insulative material (hereinafter, such a substrate is referred to as "SOI substrate"). With such a device various disadvantages and drawbacks may arise when a device element such as a transistor is formed in the monosilicon layer disposed on the electrically insulative material. These drawbacks include increase in leak current by a parasitic channel, instability of a substrate potential level, and generation of a photo-

electric leak current. Thus, a second object of the present invention is to improve the electrical characteristics of a transistor formed in the SOI substrate.

According to the present invention there is provided a semiconductor device characterised by comprising an electrically insulative layer, a monosilicon layer disposed on the insulative layer and having at least one integrated circuit formed thereon, a passivation film covering at least the integrated circuit, an adhesive layer disposed on the passivation film, and a support member fixed to the electrically insulative layer through the adhesive layer to support the monosilicon layer.

The present invention also provides a method of producing a semiconductor device characterised by comprising: forming an SOI substrate having a single crystal semiconductor layer laminated on a temporary substrate through an electrically insulative layer forming a integrated circuit on the single crystal semiconductor layer; fixing a support member by adhesive to a surface of the integrated circuit at an opposite side to the temporary substrate; removing the temporary substrate to expose a flat surface of the electrically insulative material; and forming at least an electrode on the exposed flat surface of the electrically insulative layer.

An image projection apparatus may also be provided having a light source for irradiating at least one light valve and an optical lens for projecting an enlarged image displayed on the light valves wherein the light valves each comprise a semiconductor device as defined above.

Embodiments of the present invention will now be described with reference to the accompanying drawings, of which:

Fig. 1 is a schematic sectional diagram showing a preferred embodiment of a semiconductor device according to the present invention;

Fig. 2 is a sectional diagram showing a first embodiment of the inventive semiconductor device;

Fig. 3 is a sectional diagram showing a second embodiment of the inventive semiconductor device;

Fig. 4(A-1) to Fig. 4(B-2) are schematic diagrams showing a third embodiment of the inventive semiconductor device;

Fig. 5 is a sectional diagram showing one example of an inventive MIS transistor having a structure effective to suppress a leak current;

Fig. 6 is a sectional diagram showing an inventive MIS transistor having a channel structure of similar leak current suppression type;

Fig. 7 is a sectional diagram showing an inventive MIS transistor having another channel structure of the leak current suppression type;

Fig. 8 is a sectional diagram showing an inventive MIS transistor having a similar leak current suppression structure;

Fig. 9 is a graph showing an impurity density profile measured along the line A - B of Fig. 5;

Fig. 10 is a graph showing another impurity density profile measured along the line C - D of Fig. 6;

Fig. 11(A) to Fig. 11(D) illustrate the steps in the production of the Fig. 5 MIS transistor;

Fig. 12 is a sectional diagram showing an inventive MIS transistor having a leak current suppression structure;

Fig. 13 is a sectional diagram showing an inventive MIS transistor of the LDD type having a similar leak current suppression structure;

Fig. 14 is a sectional diagram showing an inventive complementary MIS transistor pair having a leak current suppression structure;

Fig. 15 is a schematic plan view illustrative of generation mechanism of a parasitic channel;

Fig. 16 is a sectional diagram taken along the line E - F of Fig. 15;

Fig. 17 is a schematic sectional diagram illustrative of a parasitic channel suppression structure;

Fig. 18 is a sectional diagram showing an inventive complementary MIS transistor pair having a parasitic channel suppression structure;

Fig. 19 is a sectional diagram showing another inventive complementary MIS transistor pair having a similar parasitic channel suppression structure;

Fig. 20 is a sectional diagram showing a further inventive complementary MIS transistor pair having a similar parasitic channel suppression structure;

Fig. 21 is a plan view showing bipolar action.

Fig. 22 is a sectional diagram taken along the line X - X of Fig. 21;

Fig. 23 is a plan view showing an embodiment having a structure where the substrate potential is fixed;

Fig. 24 is a sectional diagram taken along the line Y - Y of Fig. 23;

Fig. 25(A) and Fig. 25(B) are schematic general diagrams illustrative of a parastic channel generating mechanism;

Fig. 26 is a graph showing a profile of impurity boron in the vicinity of a boundary between a monosilicon layer and a dielectric material layer;

Fig. 27 is likewise a graph showing a profile of an impurity phosphorus in the vicinity of a boundary between the monosilicon layer and the dielectric material layer;

Fig. 28 is a schematic diagram illustrative of an photoelectric current generation mechanism;

Fig. 29 is an energy band diagram of the monosilicon layer;

Fig. 30 is a graph showing the relationship between a gate voltage and a drain current in the MIS transistor;

Fig. 31 is a schematic diagram showing a light valve of the active matrix type constructed by using the inventive semiconductor device;

Fig. 32 is a schematic diagram showing an image projector constructed by using the Fig. 31 light valve;

Fig. 33(A) to Fig. 33(C) illustrate the steps in the production of the inventive light valve;

Fig. 34(A) and Fig. 34(B) illustrate the steps in the production of the inventive light valve; and

Fig. 35(A) to Fig. 35(D) are schematic diagrams showing examples of SOI substrates used in the production of the inventive semiconductor device.

Fig. 1 shows a preferred embodiment including means for solving the above noted drawbacks of the prior art and for achieving the objects of the present invention. The inventive semiconductor device can be utilized, for example, as a drive substrate of an active matrix light valve. The semiconductor device has, at least, an integrated circuit formed in a single crystal silicon or monosilicon layer 2 provided on an electrically insulative material 1. The electrically insulative material 1 may be composed of, for example, a silicon dioxide layer. The semiconductor device is produced by using an SOI substrate in which the monosilicon layer 2 is provided on a monosilicon wafer (not shown in the figure) through the electrically insulative material 1 or dielectric material composed of silicon dioxide film. In the completed state shown in the figure, the monosilicon wafer is removed. The dielectric material 1 composed of silicon dioxide is initially buried between the monosilicon layer 2 and the monosilicon wafer, and is therefore called "BOX".

The integrated circuit formed in the monosilicon layer 2 is covered by a passivation film having a top layer composed of a silicon oxynitride film or a silicon nitride film 3. In this embodiment, the passivation film has a double layer structure composed of the above mentioned silicon oxynitride film or silicon nitride film 3 and a silicon dioxide film 4. A transparent adhesive layer 5 is disposed on the passivation film. The monosilicon layer 2 formed on the dielectric material 1 is fixed to and supported by a transparent support member 6 through the adhesive layer 5. Stated otherwise, the integrated circuit initially formed on the SOI substrate is transferred to the support member 6 to obtain transparency. Preferably, a levelling layer 7 is interposed between the passivation film and the adhesive layer 5.

The integrated circuit formed in the monosilicon layer 2 includes a group of pixel switch elements 8 of an active matrix display, and a driver integrated circuit 9 for driving the pixel switch elements 8. The pixel switch elements 8 and the driver integrated circuit 9 are composed of an MIS transistor of the electric field effect type having a metal/insulator/semiconductor structure. Particularly, each of the pixel switching elements 8 is composed of a P channel type MIS transistor 10. On the other hand, the driver integrated circuit 9 is comprised of complementary MIS transistors. In this preferred embodiment, an N channel type MIS transistor 11 is formed in a region of the monosilicon layer 2 having a relatively great thickness, while a P channel type MIS transistor 12 is formed in another region of the monosilicon layer 2 having a relatively small thickness. Further, the driver integrated circuit 9 is formed in a region of the monosilicon layer 2 having a relatively great thickness, while the group of the pixel switching elements 8 is formed in another region of the monosilicon layer 2 having a relatively small thickness.

According to the present invention, the passivation film having the top layer composed of the silicon oxynitride film or silicon nitride film 3, is interposed between the monosilicon layer 2 formed with the integrated circuit, and the adhesive layer 5. The silicon oxynitride film or silicon nitride film 3 has a thickness over 100 nm, so as to prevent permeation of water vapor and hydrogen gas. This suppresses degradation of electrical characteristics of the transistor and improves the reliability of the integrated circuit.

The levelling layer 7 is interposed between the passivation film and the adhesive layer 5. This levelling layer 7 is composed of, for example, silicon dioxide, which does not hinder the performance of the integrated circuit and which is chemically stable and highly reliable. The interposed levelling layer 7 is effective to improve adhesion force between the adhesive layer 5 and the passivation film. Generally, the levelling layer 7 composed of silicon dioxide has better adhesion force to the adhesive layer 5 than the silicon oxynitride film or silicon nitride film 3.

The integrated circuit formed in the monosilicon layer 2 is composed of an MIS transistor having a tiny device size which enables high integration suitable for a drive substrate of active matrix light valves of large capacity. Further, the use of the monosilicon layer as a device region achieves higher operation speed of the integrated circuit which is also particularly suitable for an active matrix light valve. The driver integrated circuit 9 is composed of complementary MIS transistors effective to reduce device area and improve integration density as well as to lower power consumption. Further, the P channel MIS transistor 10 is formed in a relatively thin region of the monosilicon layer 2, while the N channel MIS transistor 11 is formed in a relatively thick region, thereby effectively suppressing leak current. Moreover, the group of pixel switching elements 8 is composed of the P channel type transistor 10 which has a relatively small leak current as compared to an N channel type MIS transistor.

Thus, in the present invention, the integrated circuit is produced by using the SOI substrate, which can be used with ordinary IC fabrication processes of

high temperature. Further, the integrated circuit formed on the SOI substrate can be transferred to the transparent support member 6 by a single device transfer.

Fig. 2 is a schematic sectional diagram showing a first embodiment of the semiconductor device according to the present invention. This embodiment is similar to the basic structure of Fig. 1, and therefore corresponding portions are denoted by the same reference numerals to facilitate understanding.

In contrast to the Fig. 1 construction, in this first embodiment in Fig. 2 the levelling layer is eliminated. Namely, the adhesive layer 5 directly contacts the silicon oxynitride film or silicon nitride film 3 disposed as the top layer of the passivation film. Such a construction simplifies the production. Though not mentioned in Fig. 1, a rear side of the dielectric material 1 is formed with a light shielding layer 13 composed of a patterned metal film, which covers selectively the MIS transistors 10, 11 and 12 to suppress the photoelectric leak current. Additionally, although not mentioned in Fig. 1, a pixel electrode 14, composed of a patterned polysilicon film, is connected to a source region of the MIS transistor 10, which constitutes each pixel switching element 8.

Fig. 3 is a schematic sectional diagram showing a second embodiment of the inventive semiconductor device. This embodiment is similar to the Fig. 1 construction, and therefore, the same reference numerals are used for the same parts to facilitate understanding. The difference in this embodiment is that the MIS transistor 10, which constitutes the pixel switching element 8, is formed in a polysilicon layer or an amorphous layer 15, rather than the monosilicon layer 2. In this embodiment, a region of the monosilicon layer 2 on the dielectric material 1 is partly transformed into an insulating film 16, such as a silicon oxide film. The polysilicon film or amorphous silicon film 15 is formed on the insulating film 16 for forming the MIS transistor 10 as the pixel switching element. Further, the polysilicon or amorphous silicon film 15 is extended to constitute a pixel electrode.

In this embodiment, the group of pixel switching elements are composed of MIS transistors. However, the present invention is not limited to this, but the pixel switching elements may be composed of diodes. The polysilicon or amorphous silicon transistor has a smaller number of electron and hole pairs generated by light irradiation and has a shorter life of carriers, as compared to the monosilicon transistor. Polysilicon or amorphous silicon transistors are thus suitable for the drive substrate of light valves. The driver integrated circuit 9 is however composed of a monosilicon transistor in a manner similar to the Fig. 1 construction. The monosilicon transistor has a high driveability, and is therefore suitable for producing a small and fast driver integrated circuit.

Fig. 4 is a schematic diagram showing a third embodiment of the inventive semiconductor device. Parts (A-1) and (A-2) are a schematic sectional view and a plan view respectively showing one MIS transistor of the driver integrated circuit. This MIS transistor 12 is formed in the monosilicon layer 2 disposed on a dielectric material, i.e., BOX 1, (see page 6 for a definition) and is comprised of a source region S, a drain region D and a gate electrode G. The MIS transistor 12 is provided in a device region bordered by a field oxide film 17. As shown in the figure, the device region of the MIS transistor 12 has a width size W_1 and length size L_1.

Parts (B-1) and (B-2) are a sectional view and a plan view respectively of one MIS transistor 10 taken from the group of pixel switching elements 8. Similarly, the MIS transistor 10 is comprised of a drain region D, a source region S and a gate electrode G. The device region, surrounded by the field oxide film 17, has a width size W_2 and a length size L_2. In this embodiment, the surface area (ie. product of L_2 and W_2) of the MIS transistor 10, which constitutes the pixel switching element 8, is set smaller than the surface area (ie. product of L_1 and W_1) of the other MIS transistor 12 contained in the driver integrated circuit.

As described before, the monosilicon transistor has a greater photoelectric leak current as compared to the polysilicon transistor and the amorphous silicon transistor. Namely, in the monosilicon transistor, the number of electron and hole pairs generated by the light irradiation is much greater, and the life of the pairs is much longer. Particularly, the pixel switching element group is frequently exposed to light irradiation. Therefore, in order to reduce a generation area of carriers and to suppress photoelectric leak current, the size of the MIS transistor of the pixel switching element group is set smaller than that of the other MIS transistor contained in the driver integrated circuit. For the same reason, a thickness of the monosilicon layer 2 is set smaller in the device region of the MIS transistor 10, than that in the other device region of the MIS transistor 12 shown in Figs. 4(A-1) and 4(A-2).

To aid understanding of the present invention, the description will now turn briefly to the photoelectric leak phenomenon of the monosilicon transistor with reference to Figs. 28 - 30. A monosilicon layer is patterned in an island shape on the BOX. An N channel MIS transistor is formed in the pattern monosilicon layer, in which a channel region Ch is provided between a source region S and a drain region D. A gate electrode G is patterned over the channel region Ch through a gate insulating film GOX. Pairs of electrons and holes are generated in the channel region Ch upon irradiation of incident light. The holes are easily accumulated in the channel region Ch to draw electrons from the source region S held at a ground potential to thereby induce the so-called bipolar action. On the other hand, the electrons are attracted by the

drain region held at a positive potential, and are concurrently collected in a portion of a boundary between the BOX and the monosilicon layer where an energy band drops. The electrons thus eventually drift to the drain region D through the boundary path. A photoelectric current thus flows in such a manner.

Fig. 29 shows the variation of an energy band in the monosilicon layer shown in Fig. 28 with respect to the thickness. The conduction band CB falls at the boundary between the monosilicon layer S-Si of the channel region and the BOX to provide an energy band structure in which electrons tend to be stored. Because of this, the leak current tends to flow through the boundary between S-Si and BOX, particularly in the N channel transistor. Further, an energy band of the valence band VB also falls at the boundary between S-Si and BOX. Because of this, the holes are not collected in this boundary area.

Fig. 30 is a graph showing the relationship between a gate voltage V_G and a drain current I_D of the monosilicon transistor. The measurement is carried out at a constant drain voltage V_D. The dotted curve indicates the characteristic under light irradiation, and the solid curve indicates another characteristic under light shielding. As seen from the graph, the leak current increases under light irradiation, thereby hindering the ON/OFF characteristic of the monosilicon transistor.

The monosilicon MIS transistor of the thin film type formed on the dielectric material, also suffers from another problem in that leak current increases through a so-called parasitic channel, in addition to the photoelectric leak current. To aid understanding, the parasitic channel will now be discussed in conjunction with Figs. 25 - 27, before proceeding to describe several embodiments directed to suppression of the parasitic channel.

Fig. 25(A) shows a general structure of the N channel MIS transistor formed in the SOI substrate. A monosilicon layer S-Si is surrounded by a field oxide film FOX to provide a device region on a BOX. The device region is formed with a pair of source and drain regions S, D of N^+ type, and a channel region is provided therebetween. A gate electrode G is patterned over the channel region through a gate insulating film GOX. An impurity region of P^- type is provided in the monosilicon layer S-Si just under the gate electrode G.

Fig. 25(B) shows a P channel MIS transistor formed on the same SOI substrate. In the P channel structure, the drain region D and the source region S are composed of a P^+ type impurity region, and an N^- type impurity region is provided in the monosilicon layer S-Si just under the gate electrode G.

Fig. 26 shows the depth profile against density of the P- type impurity region of the N channel type MIS transistor shown in Fig. 25(A). In this case, boron is doped as a P type impurity. As seen from this profile, the boron density is abruptly reduced in the monosilicon layer S-Si around the boundary between the monosilicon layer S-Si and the BOX due to segregation of boron. Therefore, the boron density is very thin in the boundary region, thereby providing a current path of the N channel MIS transistor. Consequently, a parasitic channel is easily formed to increase the leak current.

On the other hand, Fig. 27 shows the depth profile against density in the N- type impurity region of the P channel MIS transistor shown in Fig. 25(B). In this case, phosphorus is doped as an N type impurity. As seen from this profile, the phosphorus density is increased in the monosilicon layer S-Si around the boundary between the monosilicon layer S-Si and the BOX due to segregation of phosphorus. Therefore, an electric path is hardly formed in the boundary region because of the relatively high density of doped phosphorus. Consequently, the P channel MIS transistor is structurally much free from a parasitic channel as compared to the N channel MIS transistor.

Similar to an ordinary MIS transistor formed in a wafer composed of a bulk monosilicon, the MIS transistor formed in the SOI substrate is subjected to a channel doping process for threshold control. For example, in the N channel transistor, a P type impurity, such as boron, having the same conductivity type as the monosilicon layer, is doped, by ion implantation, into a surface portion of the monosilicon layer having a relatively low impurity density, typically less than $1\times10^{16}cm^{-3}$. By channel doping of the P type impurity, the monosilicon layer has a relatively high impurity density of the P type in the surface portion and a relatively low impurity distribution in the internal portion. Therefore, in the N channel MIS transistor formed in the SOI substrate, the P type impurity density is lowered in the vicinity of the boundary to the BOX or buried oxide film, as compared to the surface portion. Further, the use of boron as an impurity may cause segregation at the boundary between the monosilicon layer and the BOX as mentioned before, so that the impurity density is further reduced in the monosilicon layer. Not only the N channel transistor, but also the P channel transistor contains an electric field in the boundary between the monosilicon layer and the BOX so as to form a depletion region and inversion region around the boundary. Consequently, a parasitic channel is induced in a region of the monosilicon layer adjacent to the BOX. This region has a threshold value smaller than that of the normal channel region.

Several embodiments will be described hereinafter in detail with reference to Figs. 5 - 20, directed to suppression of the parasitic channel. First, in an embodiment shown in Fig. 5, an N channel MIS transistor is formed on an SOI substrate in an island shape. The SOI substrate has a laminate structure in which a monosilicon layer S-Si is laminated on a sub-

strate SUB composed of silicon through a BOX. This monosilicon layer S-Si is patterned in the island shape as described above to define a device region. The N channel MIS transistor includes a P^{+-} region R composed of the monosilicon layer S-Si which contains a P type impurity, a pair of N^+ source and drain regions S, D formed in the monosilicon layer S-Si doped with a P type impurity, and a channel region Ch formed over the region R between the source and drain regions S, D. A gate electrode G is patterned over the channel region Ch through a gate insulating film GOX. The P type impurity is doped into the region R adjacent to the BOX, at a sufficient density to prevent generation of a parasitic channel between the source and drain regions S, D. In addition, an N type impurity is doped into the channel region Ch for controlling a threshold voltage.

Fig. 9 shows an impurity density profile taken along the line A - B of Fig. 5. As seen from this profile, the region R is doped with the P type impurity, the amount of which is greater than that of the prior art so as to supplement a deficiency of the P type impurity due to segregation at the boundary between S-Si and the BOX. By this, inversion of the parasitic channel can be prevented prior to the inversion of the normal surface channel, thereby avoiding inadvertent conduction between the source region S and the drain region D. Further, the N type impurity is doped into the surface channel region Ch to reduce relatively or effectively the density of the P type impurity for effecting a desired threshold control.

Fig. 6 shows another embodiment directed to suppression of the parasitic channel, and being composed of a similar N channel MIS transistor formed on the SOI substrate. In this embodiment, a region R of the monosilicon layer is composed of a P type impurity layer disposed between the gate insulating film GOX and the dielectric material BOX. The density of the P type impurity is distributed such that the region R adjacent to the BOX has a thicker density than the channel region Ch.

Fig. 10 shows a density profile of the P type impurity taken along the line C- D of Fig. 6. Likewise, in this embodiment, the density of the P type impurity is set higher in the vicinity of the boundary adjacent to the BOX so as to supplement any density decrease due to segregation. On the other hand, the density of the P type impurity is lowered in the surface channel region Ch to obtain a desired threshold characteristic. Such a density profile can be established by adjusting the acceleration energy of impurity ions in an ion implantation process.

Fig. 7 shows a P channel MIS transistor formed in the SOI substrate, corresponding to the N channel MIS transistor shown in Fig. 5. Namely, the region R of the monosilicon layer adjacent to BOX contains an N type impurity, the density of which is set greater than that of the prior art, thereby suppressing a parasitic channel. On the other hand, the surface channel region Ch has a certain density of the P type impurity, which is lower than that of the rest of the region R to obtain a desired threshold characteristic.

Fig. 8 shows likewise a P channel MIS transistor formed on the SOI substrate, which corresponds to the N channel MIS transistor shown in Fig. 6. Namely, in this embodiment, the region R of the monosilicon layer adjacent to BOX contains an N type impurity having a relatively high density as compared to the prior art so as to suppress a parasitic channel. On the other hand, the surface channel region Ch has a density of the N type impurity which is set lower than that of the rest of the region R to thereby obtain a desired transistor threshold characteristic.

Referring to Fig. 11 the description will now be given in detail for a method of producing the Fig. 5 embodiment. First, an SOI substrate is prepared in Step (A). In this, a SOI substrate, a monosilicon layer 103 having a thickness of less than 1 μm is provided on a silicon substrate 101 through a silicon oxide film 102 which constitutes a dielectric material or a BOX. Subsequently, a P type impurity, such as boron, is doped by ion implantation at a given impurity density (for example, $1 \times 10^{17}cm^{-3}$). The density is sufficient to avoid generation of a parasitic channel in the monosilicon layer 103. Thereafter subjecting the wafer to a diffusion and activation process. Namely, a heating process is effected to establish a substantially uniform distribution of the P type impurity density in the monosilicon layer 103.

In Step (B), the monosilicon layer 103 is selectively removed by etching to leave a transistor device region 104 to thereby effect device isolation among individual transistors. Alternatively, a LOCOS method may be adopted for the device isolation. Further, the above noted doping process of the P type impurity may be carried out after the device isolation of Step (B).

Next, in Step (C), a gate insulating film 105 of the MIS transistor is formed by a thermal oxidation method or CVD method. Thereafter, an N type impurity is doped by ion implantation into a surface area of the region previously doped with the P type impurity for the threshold control. This forms in a surface of the transistor device region 104, a channel region 106 in which the density of the P type impurity is effectively reduced. The N type impurity is preferably composed of arsenic As having a relatively small diffusion coefficient; however, phosphorus P or antimony Sb may be selected if desired.

Lastly in Step (D), a gate electrode 107 is formed by an IC process. Further, an N type impurity is doped by ion implantation at a relatively great amount in self-alignment manner, to form a pair of source region 108 and drain region 109. The channel region 106 is thus provided therebetween, doped succeedingly with P type impurity, just under the gate electrode 107.

The source and drain regions 108, 109 are composed of an N type impurity layer which contacts with the silicon oxide film 102. Internal region 110, sandwiched by these regions, is doped with a sufficient density of the P type impurity, effective to prevent generation of a parasitic channel along a boundary 113 with the silicon oxide film 102. In the channel region 106, formed between the source region 108 and the drain region 109, along a surface layer of the device region, the threshold value of the N channel MIS transistor might be excessively boosted since the internal region 110 has a relatively high impurity density of the P type impurity. In order to lower the threshold to a practical level, the N type impurity is doped to effectively reduce the density of the P type impurity in the channel region 106. In the internal region 110 except the channel region 106, the impurity density is relatively high so that a junction capacitance may be increased between the source and drain regions 108, 109, and the internal region 110. However, practically the source and drain regions 108, 109 are contacted with the silicon oxide film 102: hence the junction capacitance is not as increased when compared to the ordinary case, where the impurity density is made higher in a bulk silicon wafer. This is done so as not to hinder an operation speed of the transistor.

Fig. 12 shows still another embodiment effective to suppress the parasitic channel. An N channel MIS transistor is formed on an SOI substrate. This MIS transistor is characterized in that an impurity, of an opposite conductivity type to that of the source and drain regions, is doped into a vicinity of the boundary between the dielectric material or BOX and the monosilicon layer S-Si, and adjacent to the opposed sides of the source and drain regions S, D. Specifically, the source and drain regions S, D have a density of N type impurity in the order of 10^{20} cm^{-3}, while the internal region R between the regions S, D has a density of P type impurity in the order of 1×10^{16} cm^{-3}. Further, a region B adjacent to the source and drain regions S, D in the vicinity of the boundary between the BOX and S-Si has a density of the P type impurity in the order of 1×10^{17} cm^{-3}. In such a manner, the region B, adjacent to the regions S, D in the vicinity of the boundary, has a higher density of P type impurity than that of the internal region R, thereby efficiently suppressing a parasitic channel. This region B might suffer from the reduction in the effective density of the P type impurity due to diffusion of an N type impurity from the source and drain regions S, D.

Fig. 13 shows a still further embodiment which has basically the same construction as that of the Fig. 12 embodiment. A difference is in that the N channel MIS transistor has an LDD structure. Namely, an LDD region is formed by doping an N type impurity at a relatively low density as compared to that of the source and drain regions S, D. Each LDD region is disposed just under a side spacer SS, composed of silicon dioxide, formed on the side walls of the gate electrode G. The region B just under the LDD region has a certain density of the P type impurity, set greater than that of the internal region R, thereby effectively suppressing a parasitic channel.

Fig. 14 shows a still further embodiment for suppressing a parasitic channel, in which a pair of complementary MIS transistors are formed on an SOI substrate. A silicon oxide film BOX is formed at a thickness of several tens nm to several μm on a monosilicon substrate SUB which has a thickness of 500 - 700 μm. An N channel MIS transistor has a source region SN and a drain region DN, a depth of which can be controlled in the order of 0.3 - 0.5 μm. This N channel MIS transistor further includes a gate electrode GN composed of polysilicon, a gate insulating film GOXN composed of silicon oxide, and a P type well PW composed of a P type impurity region having a relatively low concentration.

On the other hand, the P channel MIS transistor comprises a source region SP, a drain region DP, a gate electrode GP composed of polysilicon, a gate insulating film GOXP composed of silicon oxide, and an N type well NW composed of an N type impurity region having a low concentration. These complementary transistor devices are separated from each other by a field oxide film FOX composed of silicon dioxide. In this embodiment, the P type well refers to a region of the monosilicon layer where the N channel MIS transistor is formed, while the N type well refers to another region of the monosilicon layer where the P channel MIS transistor is formed. The P type well is composed of a P type impurity region having a low concentration formed by ion implantation etc. Alternatively, when the SOI substrate has a monosilicon layer initially containing a P type impurity and a new P type impurity may not be doped by ion implantation or diffusion, a P type well may be defined in a region where an N channel MIS transistor is formed. The same is true for the definition of the N type well.

In the Fig. 14 embodiment, the bottom of the source and drain regions SN, SD of the N channel MIS transistor does not contact with BOX. Stated otherwise, the bottom is spaced from the boundary between the BOX and PW, where an inversion layer or a depletion layer might be induced, thereby avoiding generation of a parasitic channel. Further, the bottom of the source and drain regions SP, DP of the P channel MIS transistor also does not contact the BOX. In addition, the bottom of the field oxide film FOX does not contact with the BOX.

Fig. 15 is a plan view showing the N channel MIS transistor formed on the BOX. The source region SN and the drain region DN are separated at opposite sides by the gate electrode GN, composed of polysilicon, containing a high density of N type impurity. The field oxide film FOX composed of thick silicon dioxide covers a surface portion except for the source

region SN, drain region DN and gate electrode G.

Fig. 16 shows a sectional structure taken along the channel widthwise direction of the N channel MIS transistor where the bottom of the field oxide film FOX contacts with the dielectric material BOX. Namely, the section is taken along the line E - F of Fig. 15. This figure shows the monosilicon substrate SUB, the dielectric material BOX, P type well PW, gate insulating film GOXN, field oxide film FOX and gate electrode GN. The source region SN and the drain region DN (not shown in the figure) are disposed forward and rearward, respectively, in the direction normal to the drawing paper, and therefore an electric current flows in the direction normal to the paper along the channel. The field oxide film FOX has an edge formed in a tapered shape called "bird's beak" BB. After forming the field oxide film FOX, a hatched portion r of a very thin monosilicon layer remains under the bird's beak BB. Normally, boron is doped as P type impurity into the P type well PW. When subjecting the monosilicon to an oxidation process, boron, existing in the vicinity of silicon surface, tends to migrate to the silicon oxide film due to the aforementioned segregation. Thus, when forming the field oxide film FOX, a considerable amount of boron is drifted from the region r of the monosilicon layer just under the bird's beak, to the field oxide film FOX. Consequently, the very thin monosilicon portion r just under the bird's beak has an impurity density of boron, which is considerably lower than that of the P type well just under the gate oxide film GOXN.

Normally, an insulated gate transistor of the field effect type has an electric path called a channel disposed under the gate insulating film. In the N channel MIS transistor, the higher the boron density in the channel region, the higher the threshold value of the gate voltage for conducting the channel. However, in the N channel MIS transistor formed on the SOI substrate, the bottom of the field oxide film FOX may contact with the dielectric material BOX as shown in Fig. 16. The portion r, having a very thin boron density, is formed to thereby lower the threshold value at that portion. Additionally, when the bottom of the source and drain regions contacts with the BOX, this portion r of very low boron concentration may constitute a parasitic current path. The portion r under the bird's beak BB shown in Fig. 16 corresponds to the hatched portion r in Fig. 15. The portion r is positioned widthwise of the sides of the N channel MIS transistor to form a parasitic channel to thereby increase the leak current.

In order to eliminate such a parasitic channel, the bottom of the field oxide film FOX is structurally spaced from the dielectric material BOX in the aforementioned Fig. 14 embodiment. In order to make clear this point, Fig. 17 shows a section of the N channel MIS transistor of the present embodiment, taken along the channel widthwise direction. Namely, the Fig 17 structure corresponds to the Fig. 14 structure but an orthogonal section. As understood from this figure, the bottom of the field oxide film FOX is spaced from the dielectric material BOX. Accordingly, the monosilicon layer can remain at a substantial thickness under the bird's beak BB. Therefore, in the portion r under the bird's beak BB, any P type impurity of boron contained therein can be prevented from seriously reducing the density. Namely, when carrying out a LOCOS oxidation process of the monosilicon layer to form the field oxide film FOX, boron contained in the portion r under the birds beak BB migrates into the FOX, while this portion r is supplied with boron from an underlaying monosilicon portion of the P type. Consequently in this construction, a parasitic channel can be effectively eliminated widthwise along the sides of the channel of the N channel MIS transistor, in contrast to the Figs. 15 and 16 construction.

Fig. 18 shows a variation of the Fig. 14 embodiment, and corresponding references are used for corresponding parts for facilitating understanding of the embodiment. The difference is that the bottom of the source and drain regions SN, DN of the N channel MIS transistor does not contact the BOX, while the bottom of the source and drain regions SP, DP of the P channel MIS transistor contacts the BOX and also the bottom of the field oxide film FOX contacts the BOX. As long as the bottom of the source and drain regions of the N channel MIS transistor does not contact the BOX, a parasitic channel can be eliminated widthwise from the channel ends of the N channel MIS transistor even though the bottom of the field oxide film contacts the BOX. Even if the bottom of the source and drain regions of the P channel MIS transistor contacts the BOX, the P channel MIS transistor is relatively free from a parasitic channel as described before, thereby suppressing a leak current.

Fig. 19 shows another modification of the Fig. 14, embodiment, and likewise the same references are used for denoting corresponding parts for better understanding. The difference is that while the bottom of the field oxide film FOX contacts the BOX, the BOX is spaced from the bottom of the source and drain regions SN, DN of the N channel MIS transistor, and also the source and drain regions SP, DP of the P channel MIS transistor. In a manner similar to the Fig. 14 embodiment, a parasitic channel may not be produced in either of the N channel and P channel MIS transistors, thereby suppressing a leak current.

Fig. 20 is a schematic section showing a further variation of the Fig. 14 embodiment. The same reference numerals denote corresponding parts for better understanding. The difference is that the BOX is spaced from a first field oxide film FOX1 disposed in a region of the P type well PW, one half of a second central field oxide film FOX2 on the lefthand side, and source and drain regions, SN, DN of the N chan-

nel MIS transistor. On the other hand, the BOX contacts a third field oxide film FOX3 disposed in a region of an N type well NW, the other half of the second field oxide film FOX2 on the right hand side, and source and drain regions SP, DP of the P channel MIS transistor. In the modification of Fig. 20, as opposed to the embodiments shown in Figs. 14, 18 and 19, the P type well PW formed with the N channel MIS transistor is composed of a thick monosilicon layer having a thickness t_{SN} which is greater than a thickness t_{SP} of a thin monosilicon layer constituting the N type well NW formed with the P channel MIS transistor. By such a construction, the source and drain regions SN, DN of the N channel MIS transistor can be spaced from the dielectric material layer BOX. Similar to the Figs. 18 and 19 embodiments, the Fig. 20 modification is free of a parasitic channel in either of the complementary MIS transistors, thereby advantageously suppressing any leak current.

A complementary pair of MIS transistors are formed in those of the Figs. 14, 18, 19 and 20 embodiments. However, the present invention is not limited to this, but a bipolar transistor and other devices can be formed concurrently with the complementary MIS transistors. Namely, the semiconductor device according to the present invention is not limited to a so-called CMOSIC, but may include BiCMOSIC and others.

The description will now be given for embodiments directed to suppression of "bipolar action". A substrate potential of the monosilicon layer is floated in the transistor, which is formed on the SOI substrate. Therefore, holes tend to be stored in the substrate of the N channel MIS transistor, while electrons tend to be stored in the substrate of the P channel MIS transistor. The storage of these carriers in the substrates may lower a barrier height (which is an internal potential of the PN junction and is called a "built-in potential") between the source region and the substrate, so that the carriers start to flow from the source region to the substrate. Such a bipolar action is described before in conjunction with Fig. 28. The substrate potential must be fixed in order to prevent this bipolar action, and the following embodiments are directed thereto.

Prior to the description of the embodiments, brief discussion will be given for the background art in conjunction with Figs. 21, 22 to aid understanding.

Fig. 21 is a plan view showing a drive substrate utilized in a light valve of the active matrix type, and particularly showing a picture area thereof. This picture area is formed on a monosilicon layer S-Si provided on a dielectric material (not shown). Scanning lines G are formed of a polysilicon in a row direction on the surface of the drive substrate. A part thereof constitutes a gate electrode. Further, a plurality of pixel electrodes E are formed in a matrix arrangement. Each pixel electrode E is composed of a polysilicon having a thickness in the order of several tens nm, and therefore is substantially transparent. An individual transistor comprises a source region S and drain region D formed of a high density impurity layer in a monosilicon. The source region S is connected to a corresponding pixel electrode E through a contact hole CON. Further, the drain region D is connected to a signal line (not shown) composed of metal, such as aluminium, through another contact hole CON.

Fig. 22 shows a sectional structure of an individual transistor which constitutes a pixel switching element, taken along the channel lengthwise direction. Namely, the section is taken along the line X-X of Fig. 21 when the transistor is a P channel MIS transistor. This transistor is provided with an N type well W containing an N type impurity. The gate electrode G is patterned as a part of the aforementioned scanning line over the well through a gate oxide film GOX. A pair of source and drain regions S, D containing a high density P type impurity are formed on either side of the N type well W. Such a structure of the P channel MIS transistor is provided on an underlayer of silicon oxide film BOX. This transistor is surrounded by a field oxide film FOX for device isolation. The source region is connected to a pixel electrode (not shown) through a thin polysilicon film P-Si. The gate electrode G is coated by a silicon oxide film SiO_2 to provide electrical separation from the pixel electrode. The signal line SIG is composed of metal, such as aluminium, and is connected to the drain region D of the transistor. The signal line SIG is electrically insulated from the pixel electrode by an intermediate insulating film PSG.

In this embodiment, the N well W, composed of N type impurity and the source and drain regions S, D, are formed in a monosilicon layer disposed on the dielectric material BOX. As shown in the figure, the monosilicon layer has a relatively small thickness ts, such that the bottom of the source and drain regions S, D directly contacts the underlying silicon oxide film BOX. Since the thickness ts of the monosilicon layer is rather thin, the bottom of the field oxide film FOX also contacts the underlying oxide film BOX. The potential of the N type well W must be fixed in order to stably operate such a transistor construction for pixel switching. However, the N type well W is completely surrounded by the field oxide film FOX, and is therefore isolated in an island shape. Stated otherwise, a portion of the monosilicon layer which constitutes the N type well W is separated from another portion of the monosilicon layer formed with a peripheral driver circuit, and is therefore difficult to provide a substrate potential internally.

Thus, Fig. 23 shows a particular embodiment of the present invention in which a substate potential of the pixel switching transistor is fixed in the drive substrate of the active matrix type light valve. A monosilicon layer S-Si is provided on a dielectric material (not

shown), and is formed with individual pixel switching transistors. This drive substrate is formed with scanning lines G composed of polysilicon, a part of which constitutes a gate electrode of the transistor. Further, pixel electrodes E are formed of a polysilicon having a thickness of several tens nm. The transistor is provided with source and drain regions S, D composed of a high density P type impurity layer in the monosilicon layer S-Si. Another high density N type impurity region WR of the opposite conductivity type is provided in the vicinity of the drain region D. The source region S is connected to the pixel electrode E through a first contact hole CON1. The drain region D is connected to a signal line (not shown) composed of metal, such as aluminium, through a second contact hole CON2. Moreover the region WR of the high concentration N type impurity is connected to another metal lead (not shown),composed of aluminium, through a third contact hole CON3.

Fig. 24 shows a sectional structure of the pixel switching transistor, taken along the line Y-Y of Fig. 23. In this embodiment, the pixel switching element comprises the P channel MIS transistor. This transistor is formed in the N type well W containing the N type impurity. The gate electrode G is patterned as a part of the scanning line over the N type well W through a gate oxide film GOX. The N type well W is formed at opposite sides thereof with the source region S, composed of a high density p type impurity layer, and the high density N type impurity region WR of the opposite conductivity type, respectively. Further, the drain region D (not shown) is provided behind the N type impurity region WR. This transistor is formed over the underlying silicon oxide film BOX having a thickness in the order of serval hundreds nm to several µm. Its device region is isolated from other transistors by a field oxide film FOX. The source region S is connected to a pixel electrode (not shown) through a thin polysilicon film P-Si. Further, the gate electrode G composed of a polysilicon film is insulated from the pixel electrode composed of another polysilicon film by a silicon oxide film SiO_2. Further, the aluminium metal lead Al is connected to the above noted high density N type impurity region WR to provide thereto a ground potential. The aluminium lead Al is insulated from the pixel electrode by an intermediate insulating film PSG. The aluminium metal lead is extended from a peripheral driver circuit to electrically connect to the N type impurity region WR of the high density. Consequently, the N type well W adjacent to the N type impurity region WR of high density can also be stably fixed to ground potential.

Needless to say in the aforegoing embodiment, the aluminium lead may be formed of other metals.

Fig. 31 shows one embodiment of a light valve utilizing the inventive semiconductor device as a driver substrate, and specifically shows a liquid crystal light valve of the active matrix type. This light valve has a laminate structure where a drive substrate 201, composed of the inventive semiconductor device, is coupled to a counter substrate 202, composed of transparent glass, by a spacer 203, and an electro-optical material in the form of liquid crystal 204 is sandwiched between the pair of substrates. The driver substrate 201 has a multi-layer structure where an integrated circuit formed in a monosilicon layer 206 provided on a dielectric material 205 is transferred to a support member 208 by means of an adhesive layer 207. As described before, a passivation film 209 protects the integrated circuit, and a silicon oxynitride film or a silicon nitride film 210 is disposed as a top layer of the passivation film 209, thereby efficiently protecting the integrated circuit from degradation of its electrical characteristics due to water vapor and hydrogen gas contained in the adhesive layer 207. The driver substrate 201 is divided into a peripheral driver circuit area and a picture area. The picture area is formed integrally with pixel electrodes 211 arranged in a matrix and pixel switching elements 212 for driving the pixel electrodes 211. The peripheral driver circuit area is masked by a light shield film 213 from a rear face. Further, the pixel switching elements 212 are also masked by the light shielding film 213 from the rear face. The dielectric material 205 has a thickness t_2 in the peripheral driver circuit area, which is set greater than another thickness t_1 of the dielectric material disposed in the picture area. Particularly, the reduction in thickness of the dielectric material 205 of the picture area may improve the efficiency of the electric field applied to the liquid crystal 204.

An orientation film 214 is formed on a rear face over the picture area of the driver substrate 201. Further, the counter substrate 202 is provided on its inner front face with a common electrode 215 and another orientation film 216.

Fig. 32 shows an image projector utilizing the Fig. 31 light values which are of the transmission type. This image projector 301 comprises a light source 302, such as a lamp, and three light valves 303 - 305. The light source 302 illuminates the light valves 303 - 305 so that images on the respective light valves are projected divergently by an optical lens 306. In this embodiment, the three valves are arranged for respective images of three primary colours Red, Green and Blue R, G and B correspondingly.

The source light is reflected by a first mirror M1, passes through a filter 307, and is then split by a first dichroic mirror DM1 into a R component, and remaining G and B components. The R component is reflected by a second mirror M2, and thereafter passes through a condenser lens C1 to irradiate the first light valve 303. On the other hand, the G component is divided out by a second dichroic mirror DM2, and thereafter irradiates the second light valve 304 through a condenser lens C2. The last B component irradiates

the third valve 305 through a condenser lens C3. The R, G and B components passing through the respective light valves are combined together by dichroic mirrors DM3, DM4 and a mirror M3. The combination is then projected divergently by the optical lens 306.

As described before, the respective light valve is comprised of a driver substrate formed with pixel electrodes, and a driver circuit for activating the pixel electrodes according to a given signal, a counter substrate opposed to the driver substrate, and an electro-optical material layer composed of liquid crystal or other such medium disposed between the driver and counter substrates. The driver substrate includes a transparent dielectric material, a single crystal semiconductor layer formed on the transparent dielectric material, and a light shielding layer provided on a rear face of the transparent dielectric material in opposed relation to the single crystal semiconductor layer. The driver circuit contains transistor elements formed in the single crystal layer. The light shielding layer is provided to mask an active portion of each transistor element. The pixel electrodes are integrally formed in the single crystal semiconductor layer, and is electrically connected to the driver circuit. The driver circuit activates the pixel electrodes to act on the electro-optical material to control transmittance thereof to thereby function as a light valve.

The description will now turn to a method of producing a light valve in conjunction with Figs. 33 and 34. In the first step shown in Fig. 33(A), there is prepared an SOI substrate composed of a three-layer structure in which a temporary substrate 401 and a single crystal semiconductor layer 402 are laminated with each through a transparent dielectric material 403. In this embodiment, the temporary substrate 401 is composed of monosilicon having a thickness of 500 - 700 μm, the single crystal semiconductor layer 402 is composed of a thin film monosilicon having a thickness about 1 μm, and the transparent dielectric material 403 is composed of silicon dioxide having a thickness about 1 μm.

Next, in the second step shown in Fig. 33(B), a pixel electrode 404 is formed in a portion where the single crystal semiconductor layer 403 is selectively removed, or in a portion where a silicon dioxide film is selectively formed over the SOI substrate. Further, the single crystal semiconductor layer 403 is formed with a pixel switching element 405 and a driver integrated circuit 406 for selectively feeding a signal to each pixel switching element 405. Further, the driver is coated by a passivation film 407. The top layer 408 of this passivation film 407 is composed of a silicon oxynitride film or a silicon nitride film as described before.

In the third step shown in Fig. 33(C), a support member 410 is mounted through an adhesive layer 409 on the surface of the SOI substrate formed with the pixel electrodes 404 and the driver. Preferably, a levelling layer 411 is interposed between the passivation film 407 and the adhesive layer 409.

Next, in the fourth step shown in Fig. 34(A), the temporary substrate is removed to expose the transparent dielectric material 403. The removal of the temporary substrate is carried out by an etching process using the transparent dielectric material 403 as an etching stopper.

In the fifth step shown in Fig. 34(B), a through-hole 412 is formed in a given location of the exposed transparent dielectric material 403. Further, a metal film is formed entirely over the exposed transparent dielectric material 403. Subsequently in the sixth step, the metal film is patterned to form a light shielding layer 413 which covers partly or entirely the driver as well as to concurrently form an electrode pad 414. This electrode pad 414 is electrically connected to the driver through the through-hole 412 to provide an external electrode lead. Lastly, in the seventh step, though not shown in the figure, a counter substrate provisionally formed with a transparent electrode, is fixed to the rear face of the drive substrate formed with the light shielding layer, yet leaving a gap. Then, an electro-optical material is filled in the gap to complete the light valve.

Lastly, the description will now turn to the method of producing the SOI substrate used for making the semiconductor device according to the present invention. Currently, SOI substrates using monosilicon are classified into two types of wafer. The first type is produced such that oxygen atoms are ion-implanted into a monosilicon substrate at a given depth, and thereafter the substrate is annealed. This type of SOI wafer is called SIMOX. This wafer has the feature that the monosilicon of the SOI layer has very small variation of thickness. However, unless the thickness of the SOI silicon layer is less than 0.2 μm, the SIMOX wafer cannot achieve good quality of the monosilicon layer after annealing. When the monosilicon of the SOI layer has such a thin thickness, the bottom of the source and drain regions, of both the N channel and P channel MIS transistors, may contact the BOX, thereby failing to eliminate a parasitic channel.

In view of this, the present invention mainly utilizes an SOI substrate produced by a bonding method. Fig. 35(A) to Fig. 35(D) show various examples of the bonded SOI substrate. The SOI substrate shown in Fig. 35(A) is the most basic one in which a monosilicon layer 503 is bonded onto a monosilicon substrate 501 through a silicon oxide film 502.

In the SOI substrate shown in Fig. 35(B), three layers of electrically insulative material are interposed between the monosilicon substrate 501 and the monosilicon thin film 503. This electrically insulative material is composed of an intermediate silicon nitride layer 504 sandwiched by upper and lower silicon oxide layers 505, 506. The silicon nitride layer generates an internal tension strain. On the other hand, the sil-

icon oxide layer generates a compression strain. These layers are laminated with one another to cancel the tension and compression strains with each other to thereby reduce the overall stress.

In the SOI substrate shown in Fig. 35(C), double layers of silicon nitride 507 and silicon oxide 508 are interposed between the monosilicon substrate 501 and the monosilicon film 503. In a similar manner, the tension and compression strains are cancelled by each other to eliminate any bending deformation in the SOI substrate.

In SOI substrate shown in Fig. 35(D), further double layers of silicon nitride 509 and silicon oxide 510 are added to the structure of the aforementioned SOI substrate shown in Fig. 35(C).

Lastly, though not specifically referring to the drawings, the description will include basic processes of producing the inventive semiconductor device as a summary.

In the first step, a SOI substrate is formed such that a single crystal semiconductor layer is laminated on a temporary substrate through an electrically insulative material. In the second step, an integrated circuit is formed in the single crystal semiconductor layer. In the third step, a support member is fixed by adhesive to a surface of the formed integrated circuit oppositely to the temporary substrate. In the fourth step, the temporary substrate is removed to expose a flat rear face of the electrically insulative material. Lastly in the fifth step, at least an electrode is formed on the exposed flat face of the electrically insulative material.

Preferably, in the first step, a semiconductor substrate, composed of monosilicon, is fixed to the temporary substrate, composed of silicon, through the electrically insulative material, composed of silicon dioxide, by thermal pressing. Therefore, the semiconductor substrate is polished into a thin film to thereby form the SOI substrate having a monosilicon layer. Further preferably, in the first step, a silicon nitride layer is deposited on the temporary substrate composed of silicon as an underlayer, and subsequently a silicon dioxide layer is deposited by CVD to thereby form the electrically insulative material. Thereafter, the semiconductor is fixed by thermal pressing. Further, in the fourth step, the temporary substrate is removed by etching or a combination of etching and polishing by using the silicon dioxide layer or silicon nitride layer as an etching stopper. Moreover, in the third step, the support member is fixed by means of an adhesive containing mainly silicon dioxide. Alternatively, an adhesive is applied to a surface of the integrated circuit, and is then cured to form a single layer of the support member.

As described above, according to the present invention, the semiconductor device is constructed such that the integrated circuit formed in the SOI substrate is transferred to the transparent support member by means of an adhesive layer. In this structure, a silicon oxynitride film or silicon nitride film is utilized as a top layer of the passivation film for coating the integrated circuit, thereby advantageously blocking any water or hydrogen contained in the adhesive layer, to prevent degradation of the electrical characteristics of the integrated circuit to improve its reliability. Further, a levelling layer may be interposed between the adhesive layer and the passivation film when transferring the integrated circuit, thereby advantageously improving the adhesion strength. Particularly, the levelling layer can be composed of silicon dioxide material, which does not affect the integrated circuit, thereby advantageously and stably maintaining the reliability.

The inventive semiconductor device can be used as a drive substrate for a light valve of the active matrix type. In such a case, a switching transistor contained in a picture area can be composed of polysilicon or amorphous silicon, thereby advantageously suppressing any photoelectric leak current. On the other hand, the peripheral driver circuit may be composed of transistors utilizing the monosilicon as it is, thereby advantageously realizing a driver circuit having high driveability, small device size and fast operation speed.

Further, according to the present invention, an impurity having an opposite conductivity type to the source and drain regions are doped into the boundary between the monosilicon layer and the dielectric material BOX, of a relatively high density, thereby advantageously suppressing any parasitic channel. Particularly, the bottom of the source and drain regions of the N channel MIS transistor may be spaced from the underlying dielectric material, thereby advantageously preventing the parasitic channel. Similarly, the bottom of the field oxide film surrounding a device region of the N channel MIS transistor may be spaced from the underlying dielectric material, thereby advantageously eliminating the parasitic channel.

When the inventive semiconductor device is utilized as a drive substrate of the light valve, the switching transistor element formed in the picture area may be irradiated by an incident light. In view of this, the size of the pixel switching transistor is set smaller than that of the peripheral driver circuit transistor, thereby avoiding any increase in photoelectric current. Particularly, the pixel switching element can be composed of a P channel MIS transistor, which is effective to suppress any leak current, thereby advantageously improving the ON/OFF characteristic. Further, the pixel switching transistor is formed in a region where the monosilicon layer has a relatively small thickness as compared to another region of the monosilicon layer where the peripheral driver transistor is formed, thereby advantageously suppressing any leak current.

In addition, the substrate potential of the transis-

tor is fixed in the monosilicon layer, thereby advantageously supressing any leak current due to bipolar action.

According to the present invention, the SOI substrate produced by the bonding method is adopted thereby providing a semiconductor device having a low production cost and high reliability. Particularly, double layers of a nitride film and an oxide film are used as an electrically insulative material interposed between the monosilicon layer and the monosilicon substrate so that tension strain and compression strain are cancelled by each other, thereby advantageously preventing deformation of the SOI substrate.

Additionally, when the inventive semiconductor device is used as a drive substrate in the light valve, the exposed dielectric material has a relatively small thickness in the picture area, thereby advantageously generating an electric field to drive the light valve.

The aforegoing description of the present invention has been given by way of example only and it will be appreciated by a person skilled in the art that modifications may be made without departing from the scope of the present invention. Moreover, it will be appreciated that the aforegoing embodiments are not exclusive to each other and may be combined in a variety of ways.

Claims

1. A semiconductor device characterised by comprising an electrically insulative layer(1; 101, 102; 205; 403; 502), a monosilicon layer (2; 103; 206; 402; 503) disposed on the insulative layer and having at least one integrated circuit (10, 11, 12; 212; 405, 406) formed thereon, a passivation film (3, 4; 209; 407) covering at least the integrated circuit, an adhesive layer (5; 207; 409) disposed on the passivation film, and a support member (6; 208; 410) fixed to the electrically insulative layer through the adhesive layer to support the monosilicon layer.

2. A semiconductor device according to claim 1, wherein the passivation film has a top layer (3; 210; 408) comprising one of a silicon oxynitride film or a silicon nitride film.

3. A semiconductor device according to claim 1 or 2, including a levelling layer (7; 411) interposed between the passivation film and the adhesive layer.

4. A semiconductor device according to any one of claims 1, 2 or 3, in which said integrated circuit comprises a number of switching elements (10; 212; 405) and a number of drivers (11; 406), each for driving a respective switching element for use in an active matrix display.

5. A semiconductor device as claimed in claim 4, further comprising an insulative film (16) formed from said monosilicon layer and a semiconductive layer (15) disposed on said insulative film and comprising one of a polysilicon layer or an amorphous silicon layer, in which said switching elements are formed on said semiconductive layer.

6. A semiconductor device according to claim 4 or 5, wherein the switching elements and the drivers comprise a MIS transistor of an electric field effect type having a metal/insulator/semiconductor structure.

7. A semiconductor device according to claim 6, wherein the switching elements each comprise an MIS transistor of a P channel type.

8. A semiconductor device according to claim 6 or 7 when dependent on claim 5, in which each MIS transistor of the switching elements is smaller than that of the respective MIS transistor forming the driver.

9. A semiconductor device according to any one of claims 4 to 8, in which the drivers are formed in a region of the monosilicon layer having a relatively great thickness while the switching elements are formed in another region where the monosilicon layer has a relatively small thickness.

10. A semiconductor device according to any one of claims 6 to 9 when dependent on claim 6, in which each MIS transistor comprises a pair of source and drain regions a channel region (ch, 106) formed between the source and drain regions (S, D; 108 109) and a region (R) formed under said channel region.

11. A semiconductor device according to claim 10, wherein the source and drain regions are spaced apart from the electrically insulative layer.

12. A semconductor device according to claim 10 or 11, in which said region includes an impurity of a first electroconductivity type, said source and drain regions contain another impurity of a second electroconductivity type and wherein an impurity of the first electroconductivity type is doped between the source and drain regions at a certain density sufficient to suppress generation of a parasitic channel, and another impurity of the second electroconductivity type is doped into the channel region for controlling a threshold voltage.

13. A semiconductor device according to claim 10 or 11, in which said region includes an impurity of a first electroconductivity type, said source and drain regions contain another impurity of a second electroconductivity type and wherein a gate electrode (G; 107) is disposed on the channel region through a gate insulating film (GOX; 105), and wherein a part of the region positioned between the gate insulating film and the electrically insulative layer comprises an impurity layer (106) of one electroconductivity type, having a relatively thin density in the channel region as compared to a lower region in the vicinity of a boundary (113) to the electrically insulative material.

14. A semiconductor device according to claim 10, 11, 12 or 13, further including an impurity region (B) having an opposite electroconductivity type to that of source and drain regions, and being formed in the vicinity of a boundary between the electrically insulative layer and the monosilicon layer at locations adjacent to the source and drain regions.

15. A semiconductor device according to any one of claims 6 to 14, in which an N type MIS transistor is formed in one of a P type impurity region and a P well region (PW) which includes a field oxide film (FOX, 17) spaced apart from the electrically insulative layer.

16. A semiconductor device according to any one of claims 4 to 15, wherein each switching element has, around its vicinity, a high impurity region having the same electroconductivity type as that of a substrate composed of the monosilicon layer.

17. A method of producing a semiconductor device characterised by comprising: forming an SOI substrate (101, 102; 205; 501) having a single crystal semiconductor layer (2,103; 206; 402; 503) laminated on a temporary substrate (101; 401) through an electrically insulative layer (1; 102; 205; 403; 502) forming a integrated circuit (10, 11, 12; 212; 405, 406) on the single crystal semiconductor layer; fixing a support member (6; 208; 410) by adhesive (5; 207; 409) to a surface of the integrated circuit at an opposite side to the temporary substrate; removing the temporary substrate to expose a flat surface of the electrically insulative material; and forming at least an electrode (14; 211; 404) on the exposed flat surface of the electrically insulative layer.

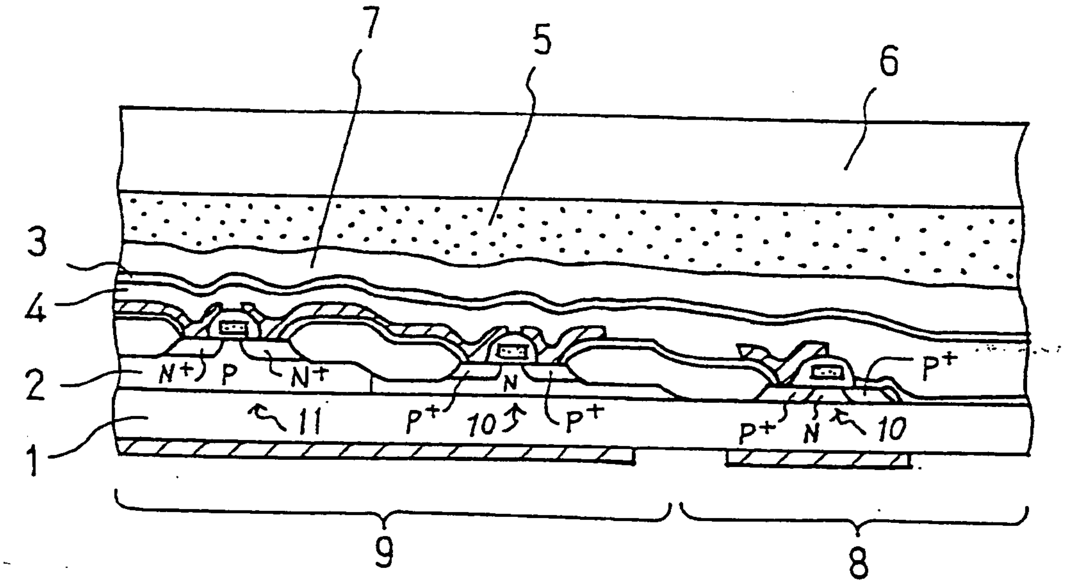
18. A method of producing a semiconductor device according to claim 17, wherein forming the SOI substrate comprises fixing the single crystal semiconductor layer by thermal adhesion to the temporary substrate, through the electrically insulative layer, and thinning the semiconductor layer to form the SOI substrate having the single crystal layer.

19. A method of producing a semiconductor device according to claim 17, wherein forming the SOI substrate includes forming the electrically insulative layer by depositing a silicon nitride layer (504; 507; 509) as an underlayer on the temporary substrate, depositing a silicon dioxide layer (505, 506; 508; 510) by CVD, and fixing the semiconductor substrate to the silicon dioxide layer by thermal adhesion.

20. A method of producing a semiconductive device according to claims 17 to 19, further including opening a through-hole (412) in a given position of the exposed electrically insulative layer and forming a metal film (13; 414) on the exposed surface thereof; patterning the metal film to form a mask (413) layer which covers partly or entirely one of the integrated circuits, and concurrently forming an electrode pad which electrically connects to the integrated circuit through the through-hole; coupling a counter substrate (202) formed with a transparent electrode, to a surface of the insulative layer formed with the mask layer, leaving a gap, and filling an electro-optical material (204) in the gap.

21. An image projection apparatus (301) having a light source (302) for irradiating at least one light valve (303, 304, 305), and an optical lens (306) for projecting an enlarged image displayed on the light valve(s), wherein the light valves each comprise a semiconductor device as claimed in any one of claims 1 to 16.

FIG. 1



1 dielectric material

2 monosilicon layer

3 silicon oxynitride film or silicon nitride film

5 adhesive layer

6 support member

7 leveling layer

8 pixel switching element group

9 driver integrated circuit

FIG. 2

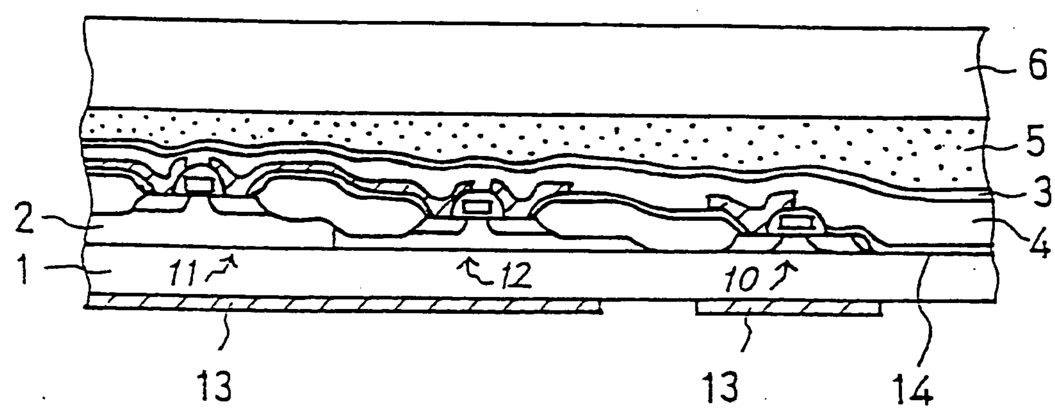


FIG. 3

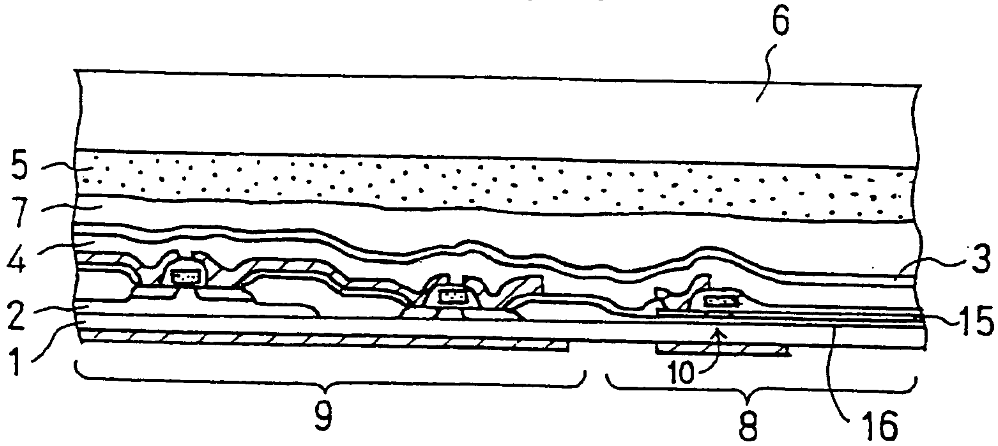


FIG. 4 (A-1)

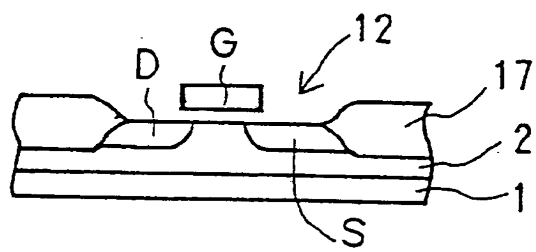


FIG. 4 (A-2)

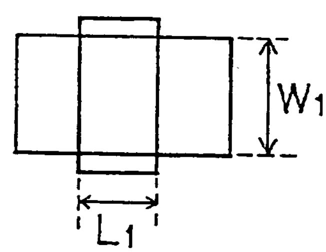


FIG. 4 (B-1)

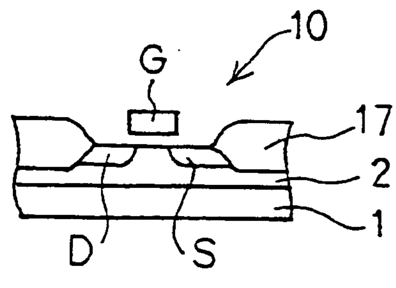
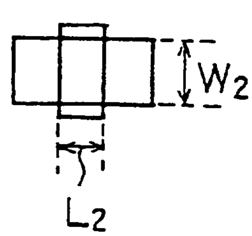


FIG. 4 (B-2)



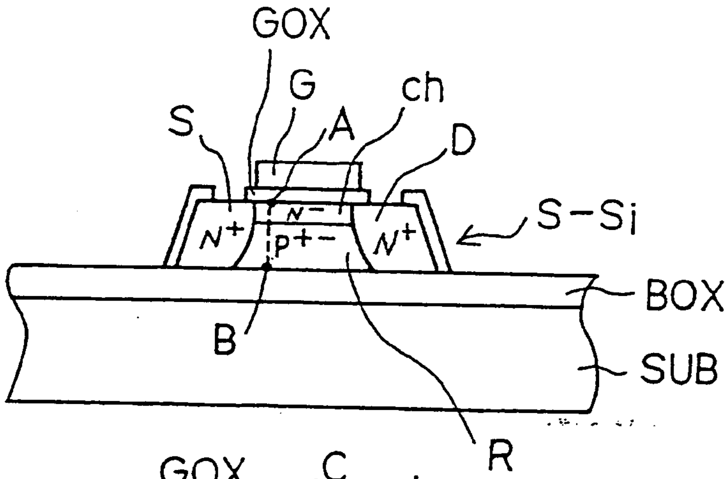


FIG. 5

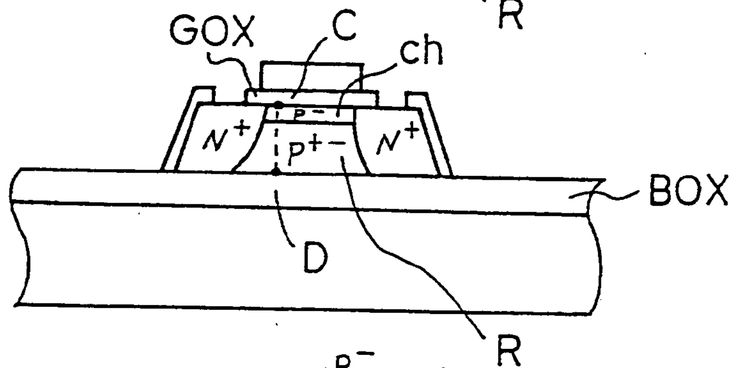


FIG. 6

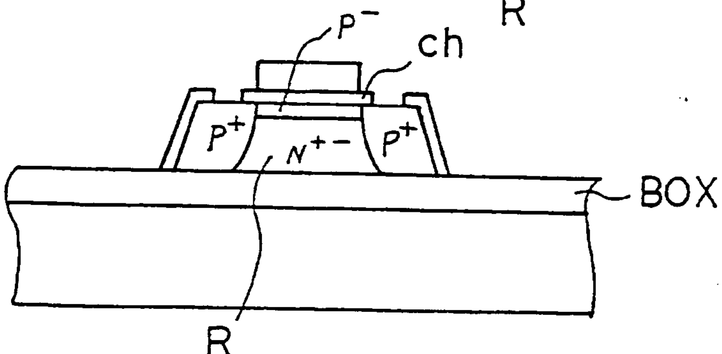


FIG. 7

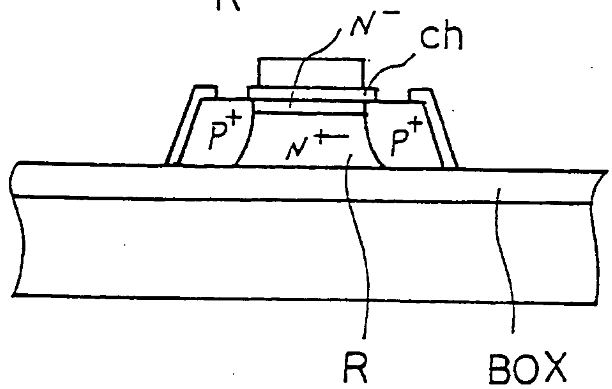


FIG. 8

FIG. 9

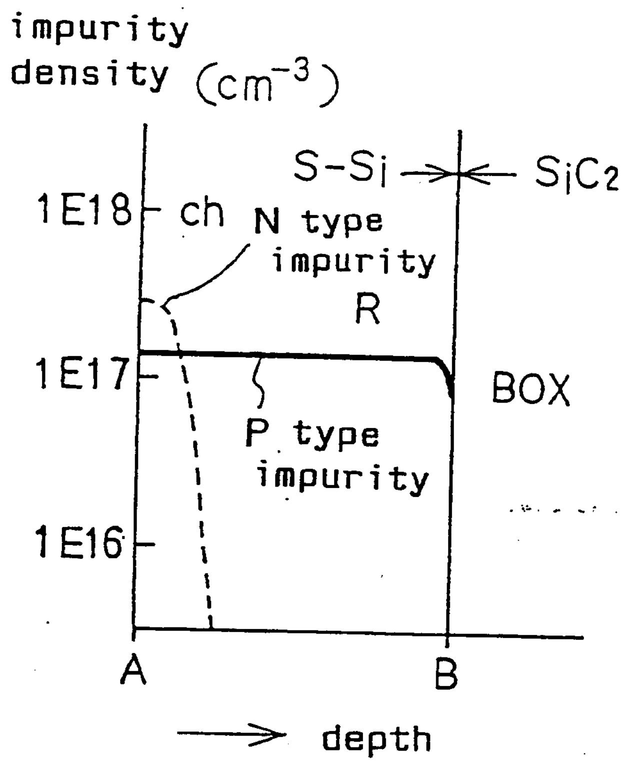

impurity
density (cm^{-3})
S-Si
SiC2
1E18
1E17
1E16
ch
N type
impurity
R
BOX
P type
impurity
A
B
depth

FIG. 10

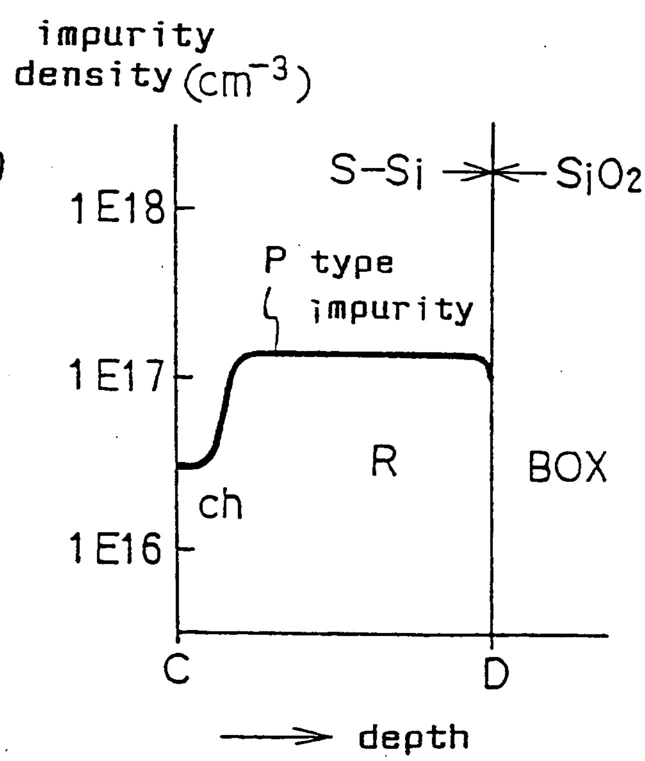

impurity
density (cm^{-3})
S-Si
SiO2
1E18
1E17
1E16
P type
impurity
R
BOX
ch
C
D
depth

FIG. 11(a)

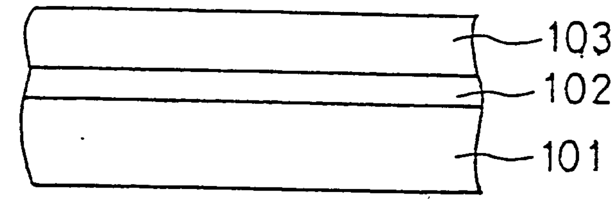


FIG. 11(b)

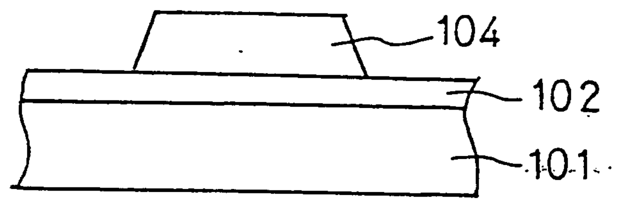


FIG. 11(c)

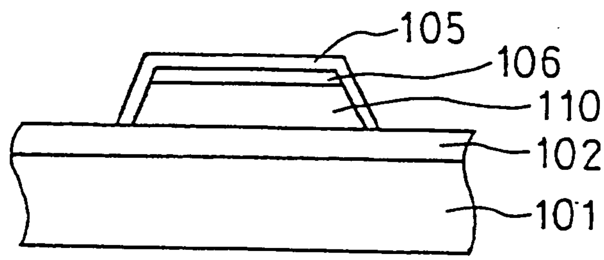


FIG. 11(d)

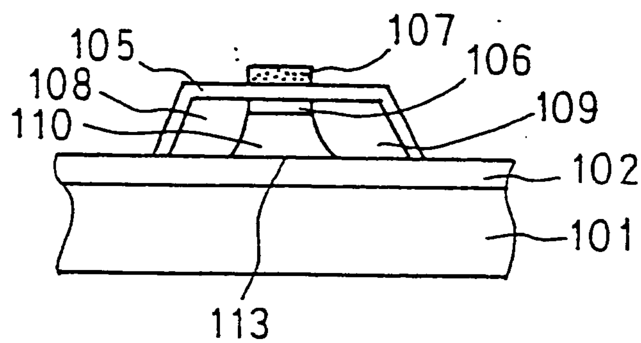


FIG. 12

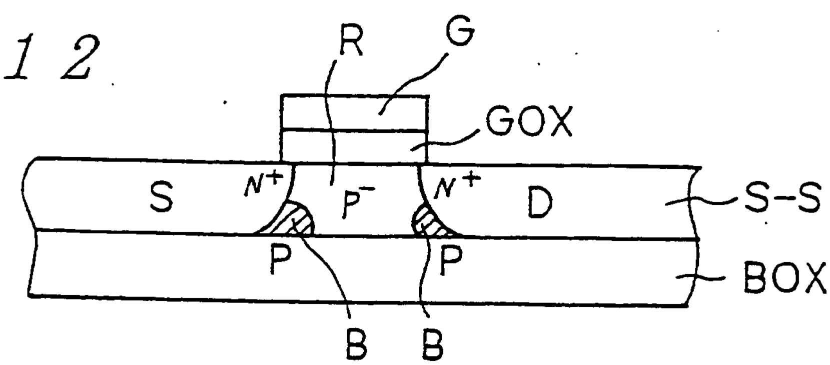


FIG. 13

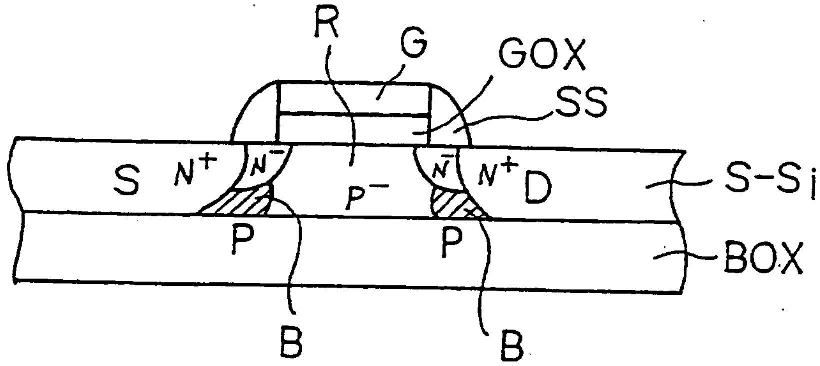

R
G
GOX
SS
S
N^+
N^-
P^-
N^-
N^+
D
S-Si
P
P
BOX
B
B

FIG. 14

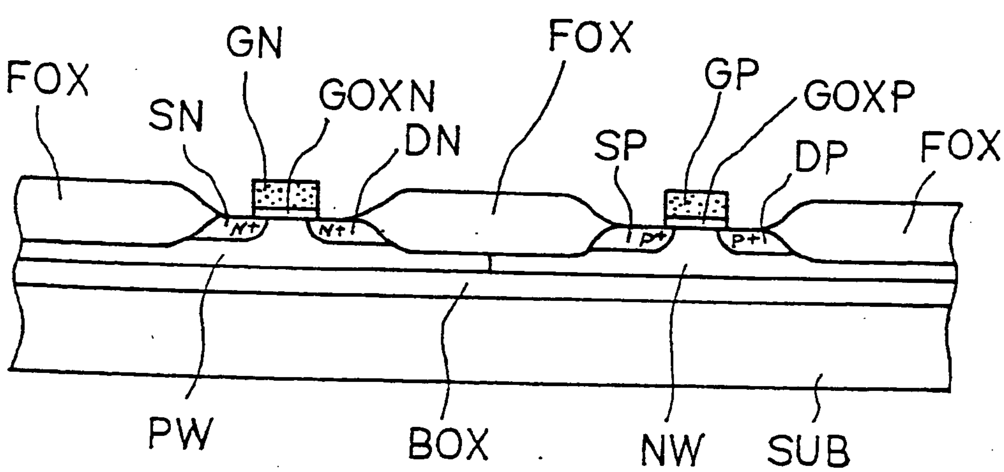

FOX
GN
SN
GOXN
DN
FOX
GP
GOXP
SP
DP
FOX
N+
N+
P+
P+
PW
BOX
NW
SUB

FIG. 15

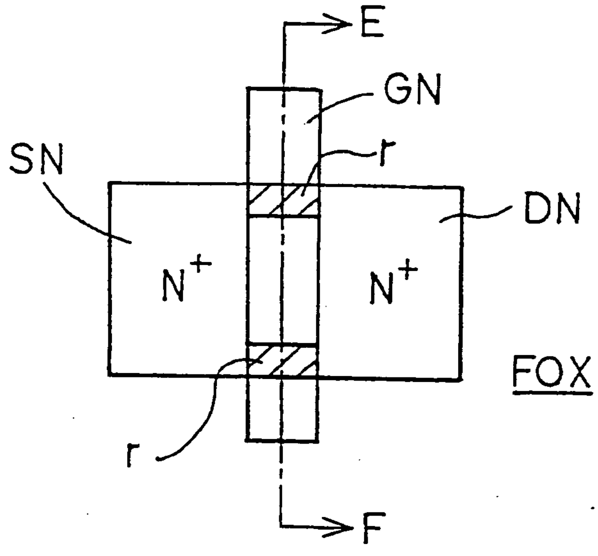


FIG. 16

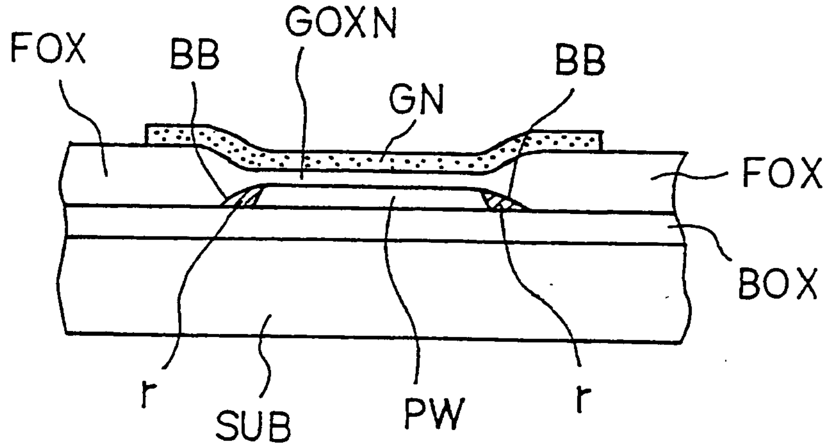


FIG. 17

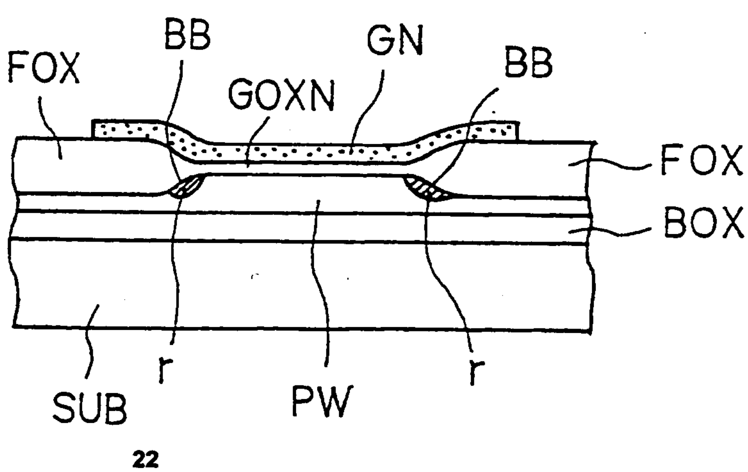


FIG. 18

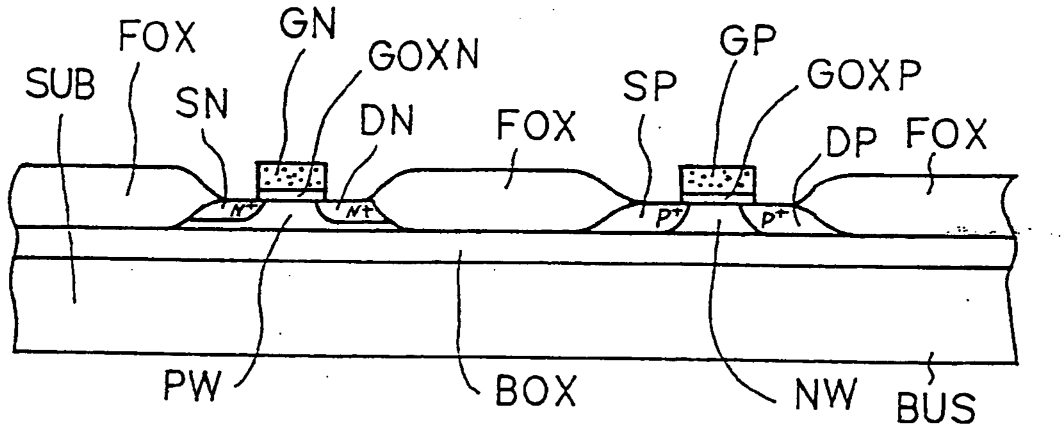

SUB
FOX
SN
GN
GOXN
DN
FOX
SP
GP
GOXP
DP
FOX
N+
N+
P+
P+
PW
BOX
NW
BUS

FIG. 19

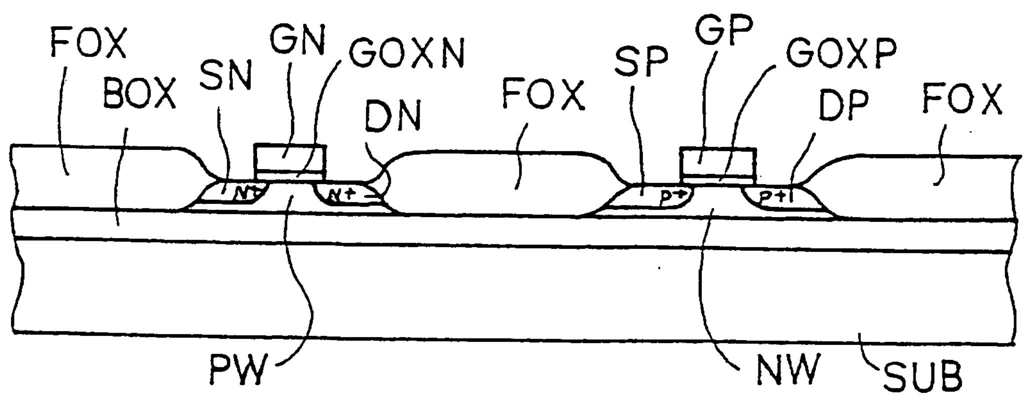

FOX
BOX
SN
GN
GOXN
DN
FOX
SP
GP
GOXP
DP
FOX
N+
N+
P+
P+
PW
NW
SUB

FIG. 18

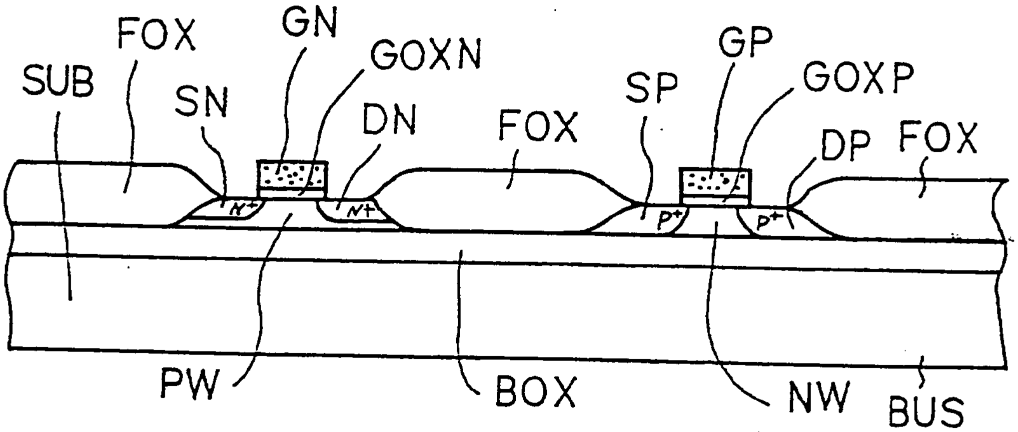

SUB
FOX
SN
GN
GOXN
DN
FOX
SP
GP
GOXP
DP
FOX
N+
N+
P+
P+
PW
BOX
NW
BUS

FIG. 19

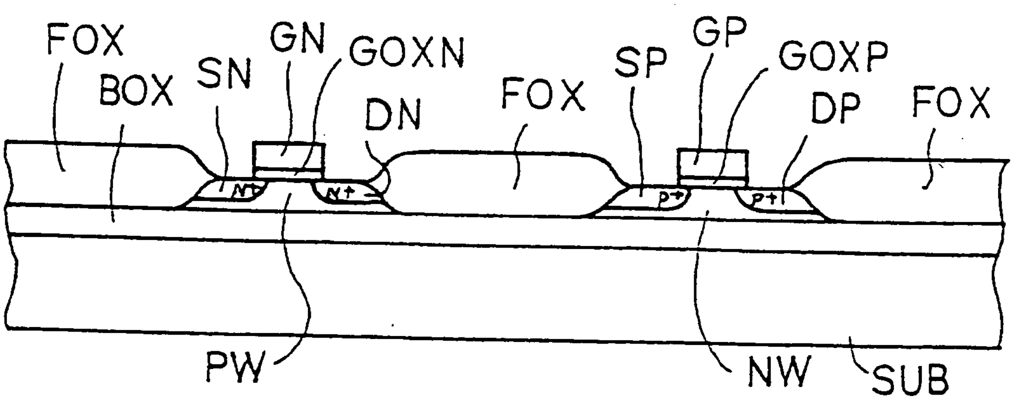

FOX
BOX
SN
GN
GOXN
DN
FOX
SP
GP
GOXP
DP
FOX
N+
N+
P+
P+
PW
NW
SUB

FIG. 20

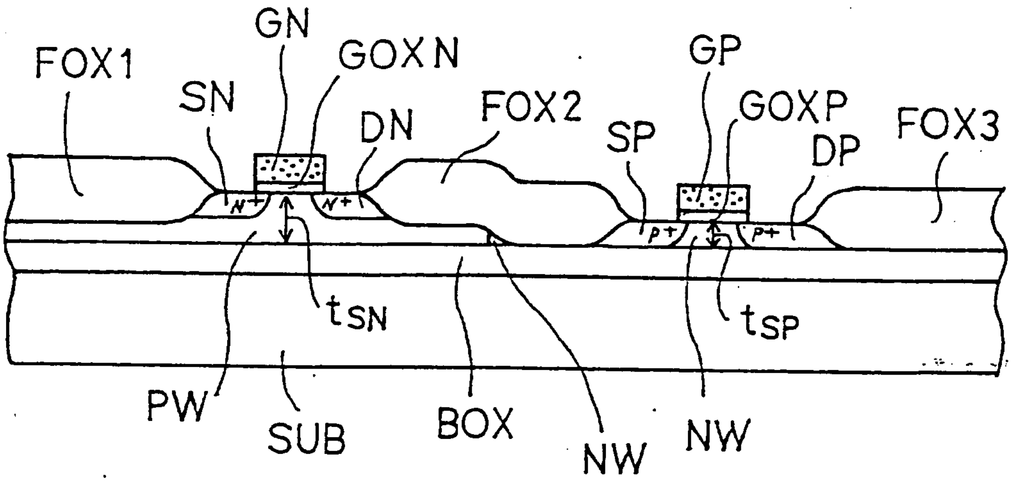

FOX1
GN
GOXN
SN
DN
FOX2
GP
SP
GOXP
DP
FOX3
N+
N+
P+
P+
tSN
tSP
PW
SUB
BOX
NW
NW

FIG. 21

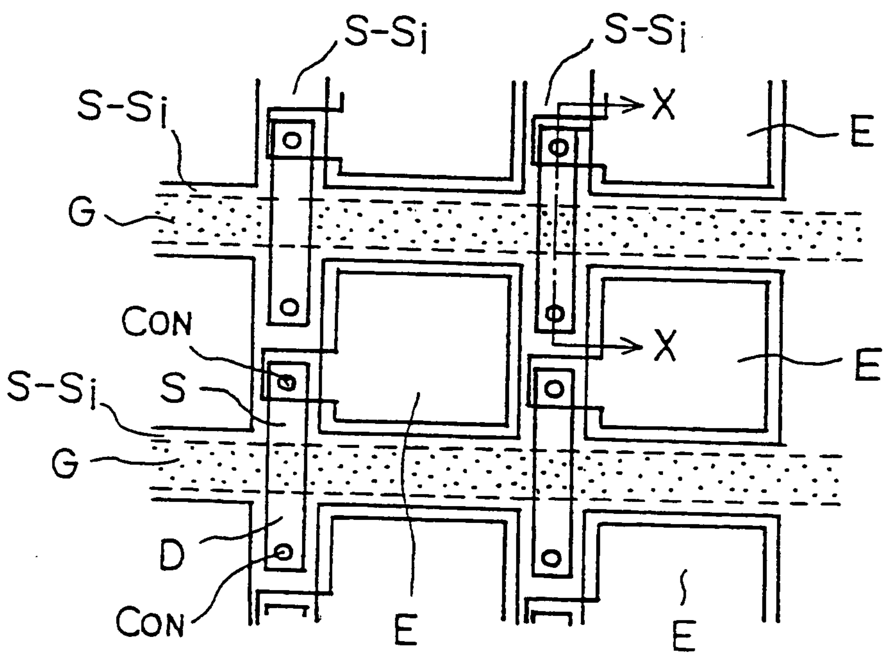

S-Si
S-Si
S-Si
X
E
G
CON
X
E
S-Si
S
G
D
CON
E
E

FIG. 22

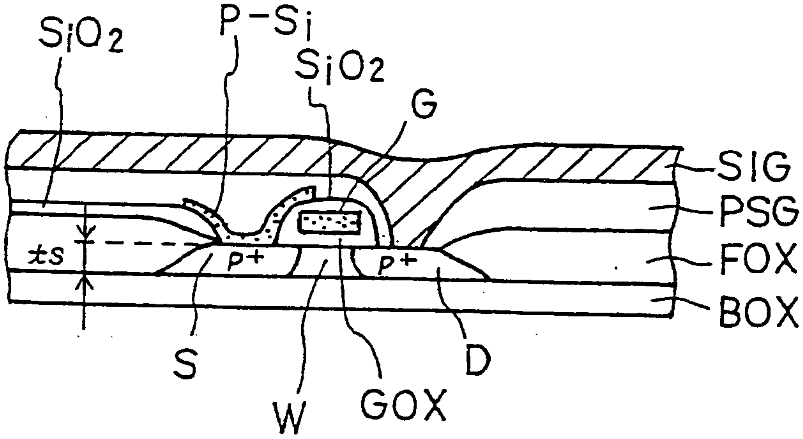

SiO2
P-Si
SiO2
G
SIG
PSG
FOX
BOX
ts
P+
P+
S
W
GOX
D

FIG. 23

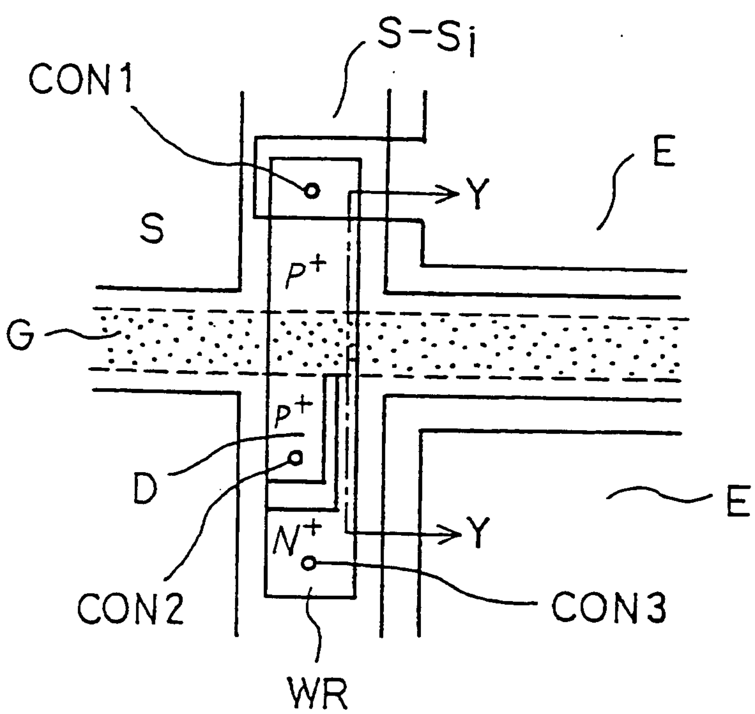
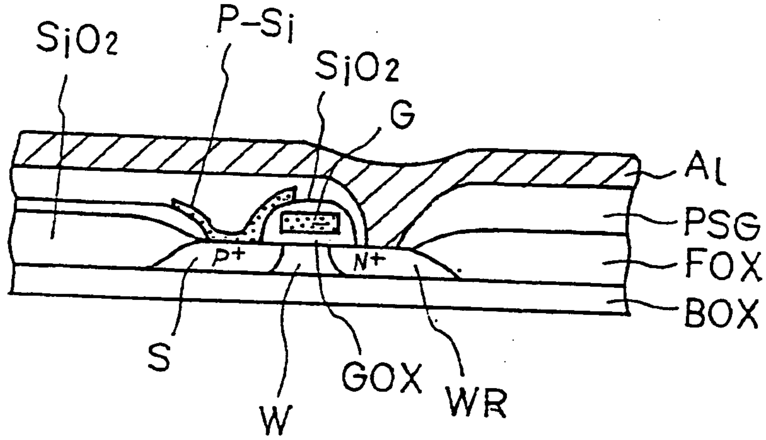

S-Si
CON1
Y
E
S
P+
G
P+
D
E
N+
Y
CON2
CON3
WR

FIG. 24



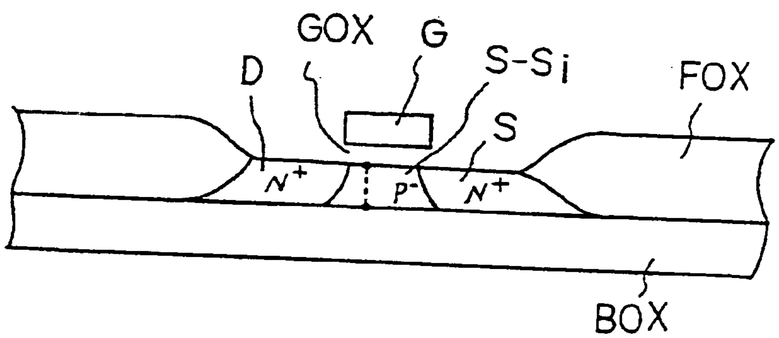


FIG. 25(a)

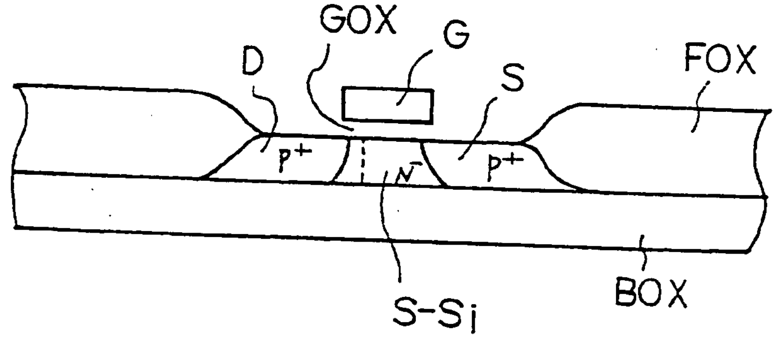


FIG. 25(b)

FIG. 26

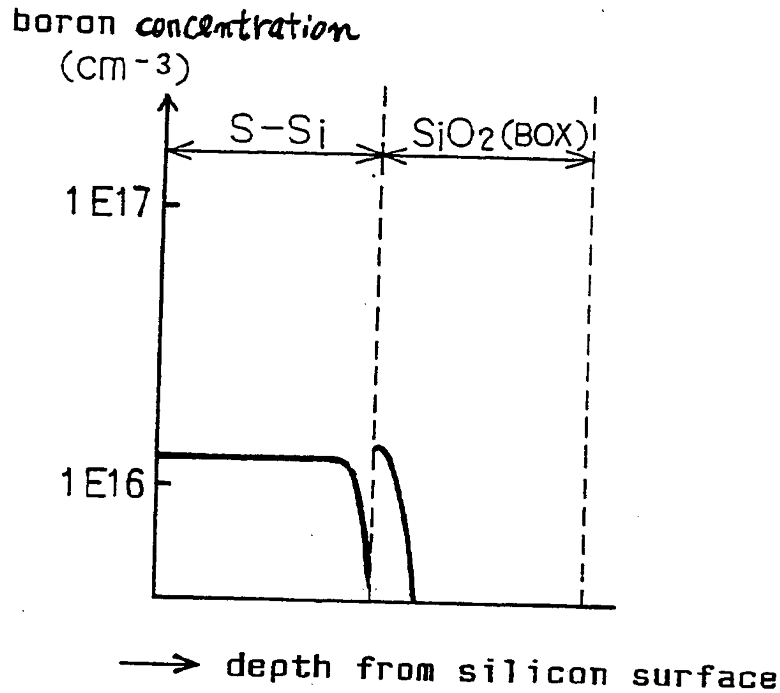

boron concentration
(cm-3)
S-Si
SiO2 (BOX)
1E17
1E16
depth from silicon surface

FIG. 27

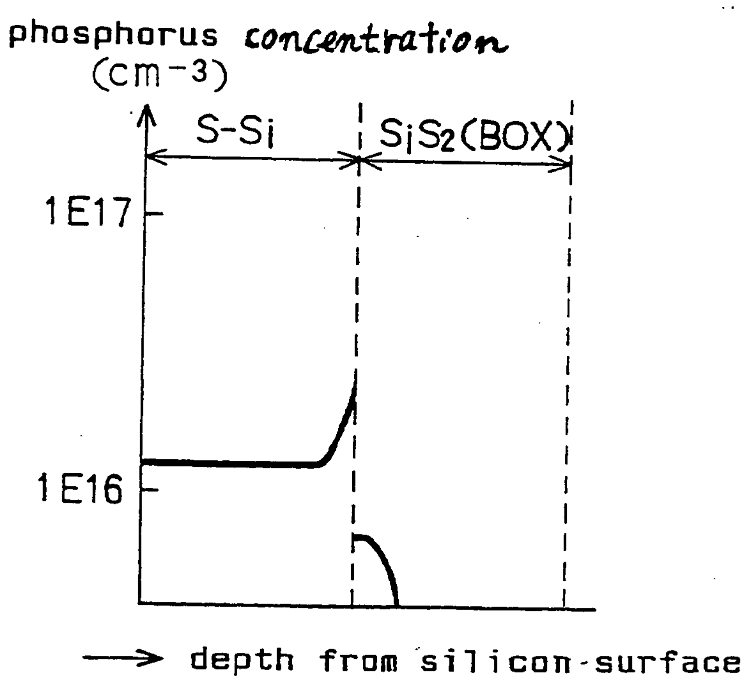

phosphorus concentration
(cm-3)
S-Si
SiS2 (BOX)
1E17
1E16
depth from silicon-surface

FIG. 28

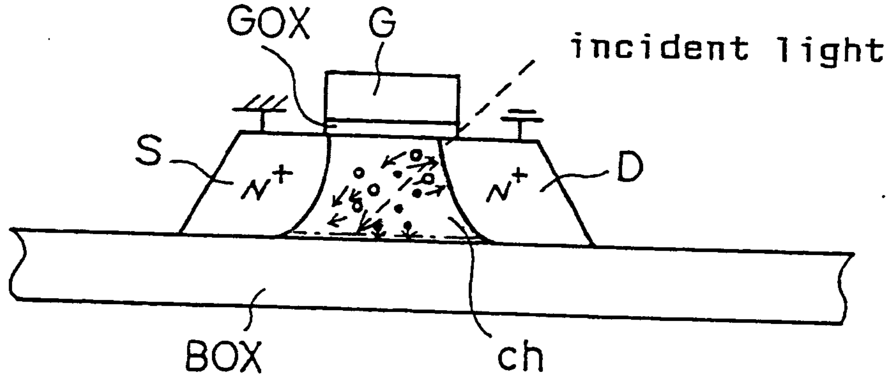


FIG. 29

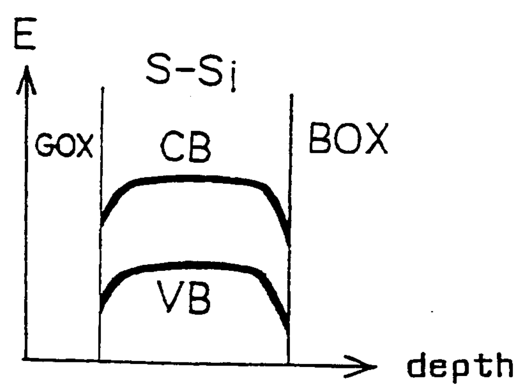


FIG. 30

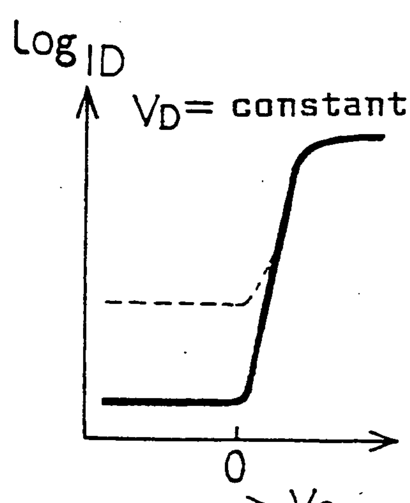
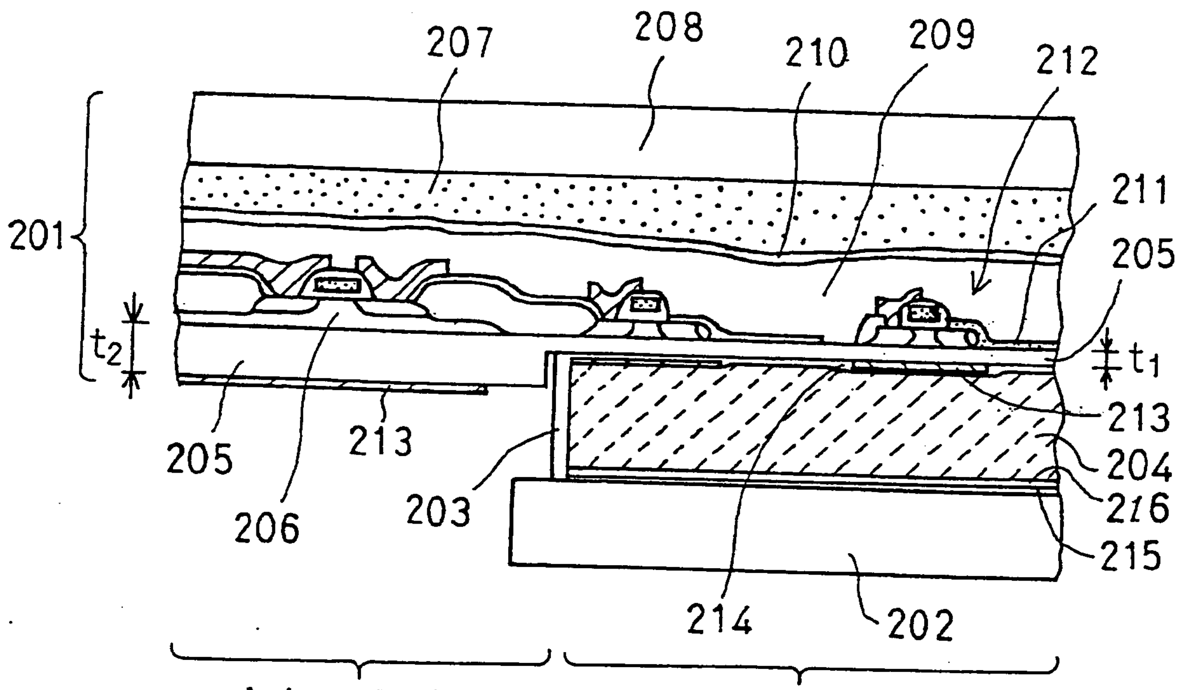
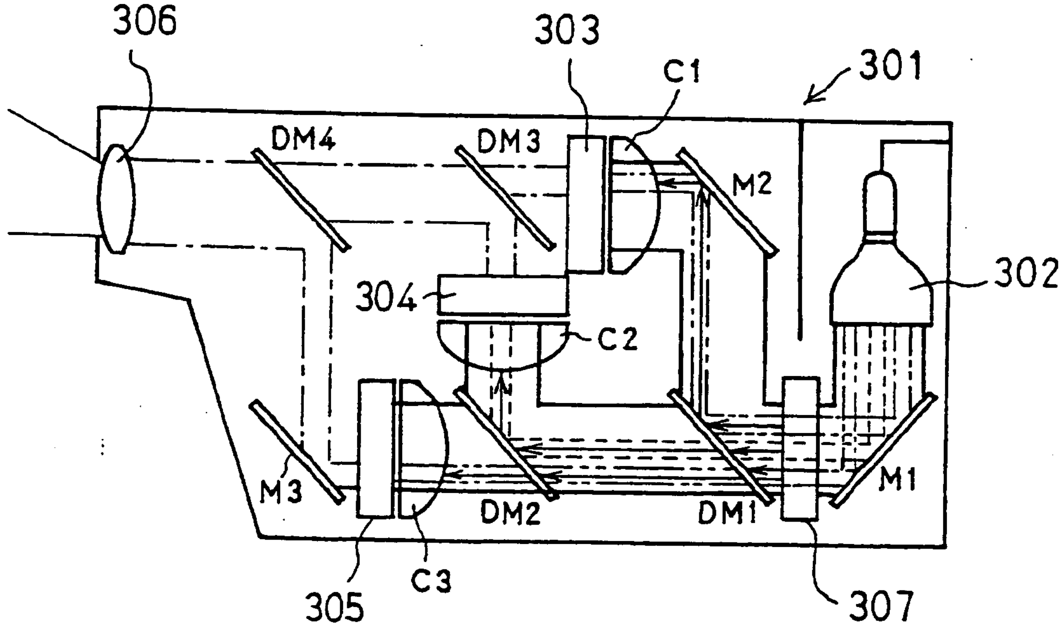


FIG. 31



201
207
208
210
209
212
211
205
t2
t1
213
204
216
215
205
213
206
203
214
202
peripheral driver circuit area
picture atea

FIG. 32



306
303
C1
301
DM4
DM3
M2
302
304
C2
M3
DM2
DM1
M1
305
C3
307

FIG. 33 (a)

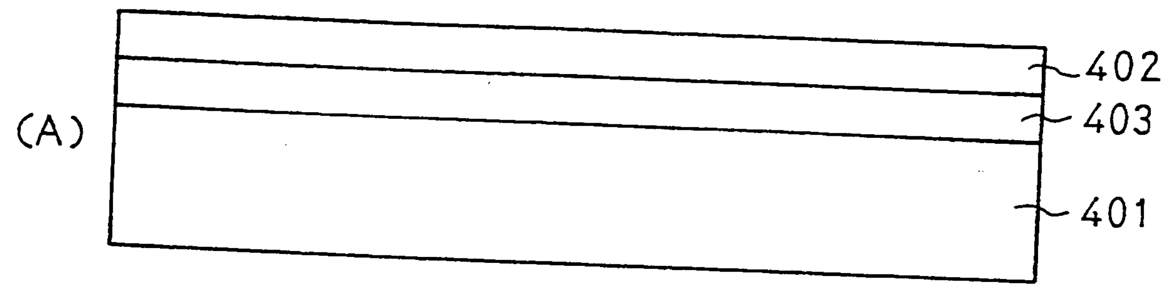


FIG. 33 (b)

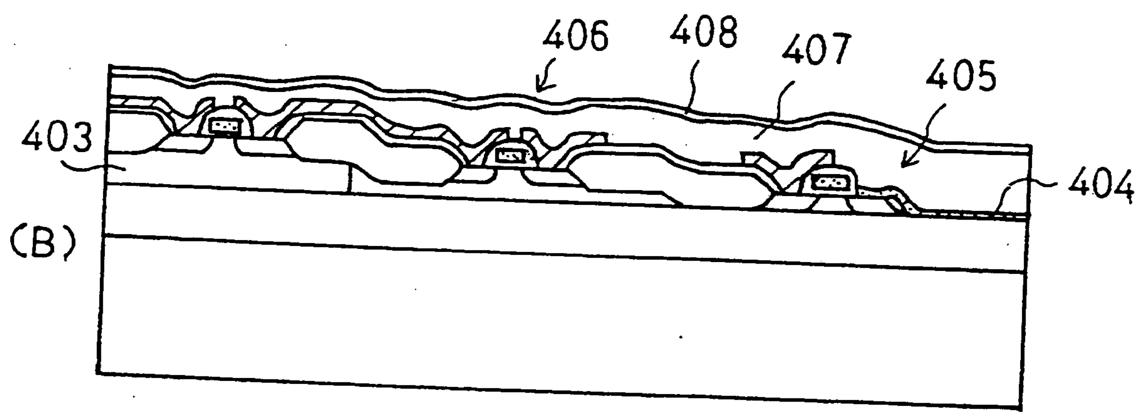


FIG. 33 (c)

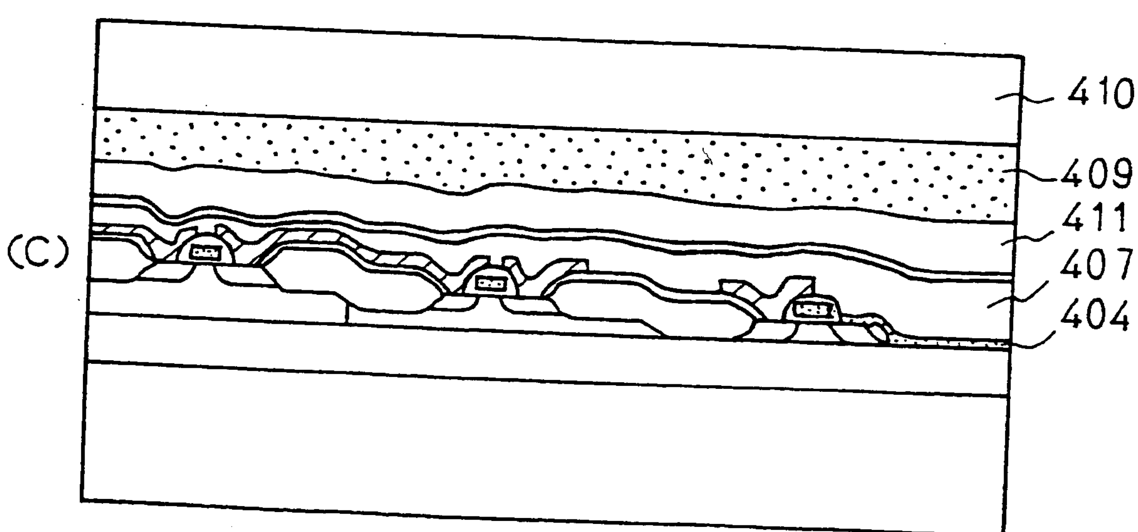


FIG. 34 (a)

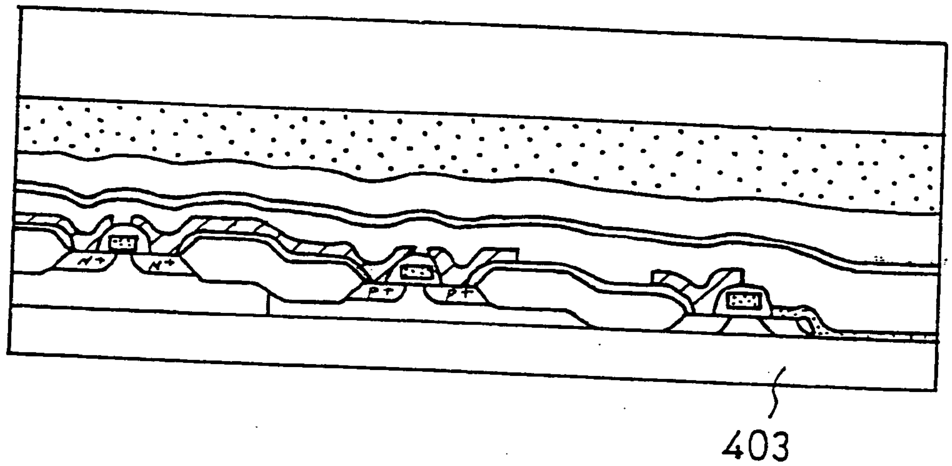
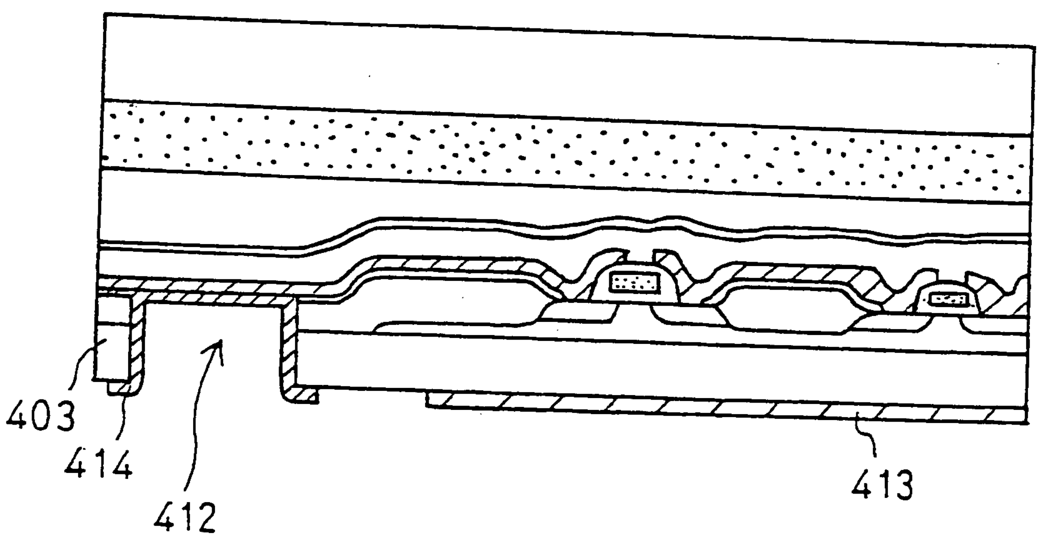


FIG. 34 (b)



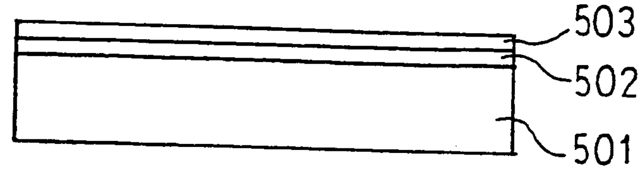


FIG. 35 (a)

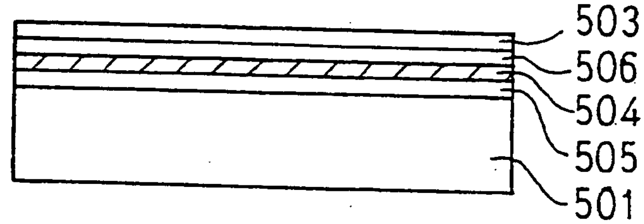


FIG. 35 (b)

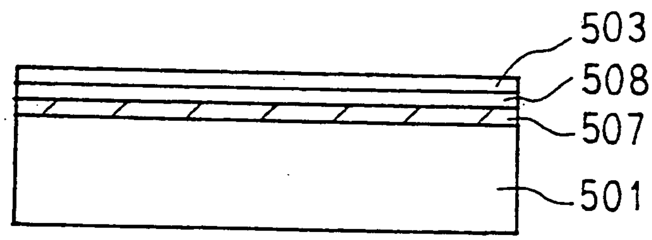


FIG. 35 (c)

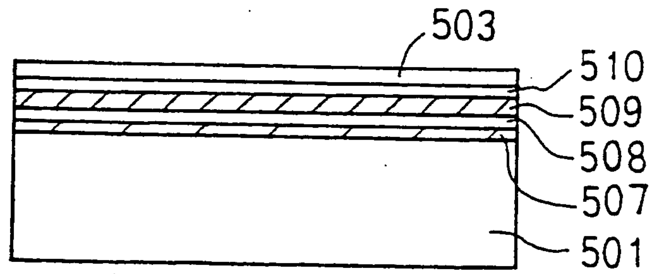


FIG. 35 (d)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 30 3657
Page 1

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
D,X	PATENT ABSTRACTS OF JAPAN vol. 12, no. 328 (E-654)6 September 1988 & JP-A-63 090 859 (NEC CORP)	1	H01L27/12 G02F1/136 H01L29/784
D,Y	* abstract *	2-7,9, 11,21	
Y	EP-A-0 182 371 (MATSUSHITA ELECTRIC INDUSTRIAL CO.,LTD.) * abstract *	2-7,9,11	
A		1,8,10, 12-21	
Y	EP-A-0 474 474 (SEIKO INSTRUMENTS INC.)	4-7,9, 11,21	
A	* abstract; claims 1-20; figures 1-8,12-21 * * figures 35-66,84 *	1-3,8, 10,12-20	
X	PATENT ABSTRACTS OF JAPAN vol. 16, no. 32 (P-1303)27 January 1992 & JP-A-32 42 622 (FUJITSU LTD)	17	
Y	* abstract *	18,19	TECHNICAL FIELDS SEARCHED (Int. Cl.5)
A		1-16,20, 21	H01L G02F
Y	PATENT ABSTRACTS OF JAPAN vol. 11, no. 77 (E-487)(2524) 7 March 1987 & JP-A-61 232 661 (TOSHIBA CORP) * abstract *	18,19	
Y	PATENT ABSTRACTS OF JAPAN vol. 8, no. 250 (E-279)16 November 1984 & JP-A-59 126 639 (NIPPON DENKI KK) * abstract *	19	
A	EP-A-0 268 380 (NEC CORP) * abstract *	1-21	

-/--

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	17 SEPTEMBER 1993	ONSHAGE A.C.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 30 3657
Page 2

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP-A-0 304 811 (ASEA BROWN BOVERI AB) * the whole document * ---	10-12	
A	US-A-4 199 773 (GOODMAN ET AL.) * abstract * ---	10	
A	PATENT ABSTRACTS OF JAPAN vol. 16, no. 210 (E-1203)19 May 1992 & JP-A-40 34 979 (SEIKO INSTR INC) * abstract * ---	11	
A	WO-A-8 808 202 (GENERAL ELECTRIC COMPANY) * abstract * ---	14	
D,A	PATENT ABSTRACTS OF JAPAN vol. 12, no. 341 (P-758)13 September 1988 & JP-A-63 101 831 (NEC CORP) * abstract * ---	20	
A	PATENT ABSTRACTS OF JAPAN vol. 10, no. 1 (E-371)(2058) 7 January 1986 & JP-A-60 167 364 (MATSUSHITA DENSHI KOGYO K.K.) * abstract * -----	1-21	TECHNICAL FIELDS SEARCHED (Int. Cl.5)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	17 SEPTEMBER 1993	ONSHAGE A.C.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)